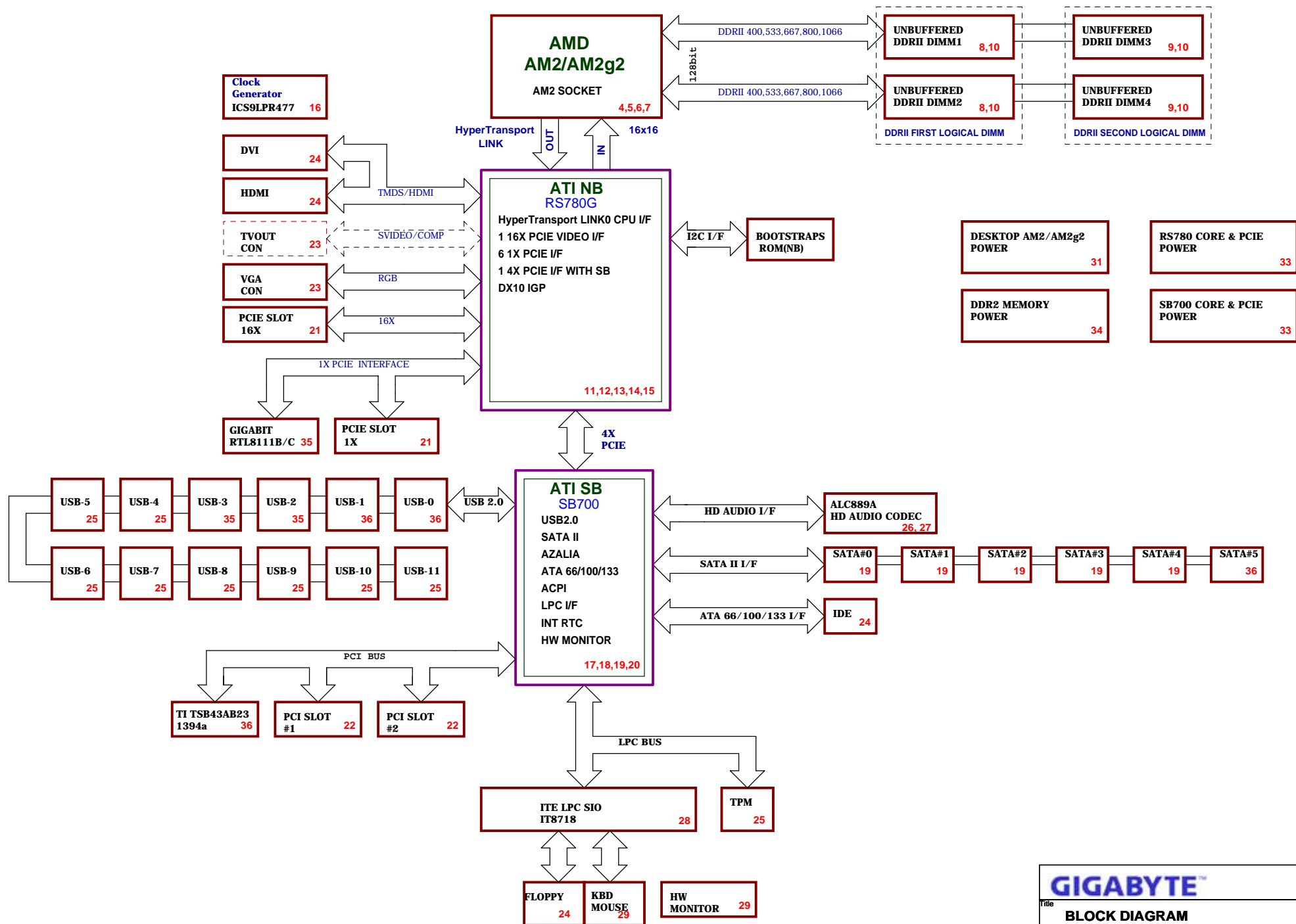


Revision : 1.0

PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRII CHANNEL A
09	DDRII CHANNEL B
10	DDRII TERMINATOR
11	RS780 HT-LINK I/F
12	RS780 PCIE I/F
13	RS780 SYSTEM I/F
14	RS780 STRAP
15	RS780 POWER & GND
16	ICS9LPRS477
17	ATI SB700 PCIE/PCI/CPU/LPC
18	ATI SB700 ACPI/USB/GPIO/AUDIO
19	ATI SB700 SATA/SPI/IDE/HWM
20	ATI SB700 POWER & GND
21	PCI EXPRESS x16 ,x1
22	PCI SLOT 1, 2
23	RGB ,TV Connector
24	IDE ,FDD ,HDMI ,DVI Connector
25	COM/LPT/F_USB

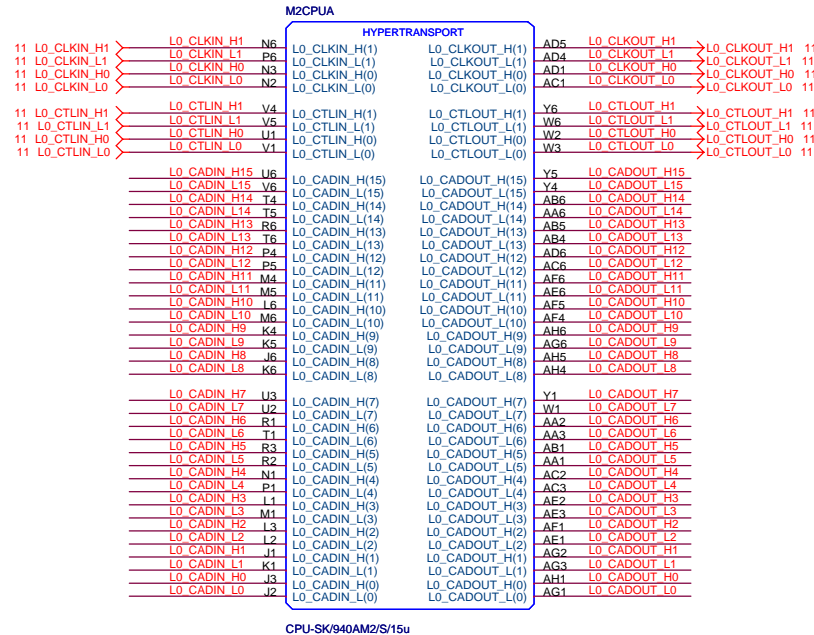
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RS780 CUSTOMER DESKTOP REFERENCE DESIGN



L0_CADIN_L[0..15] L0_CADIN_L[0..15] 11
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 11

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 11
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 11

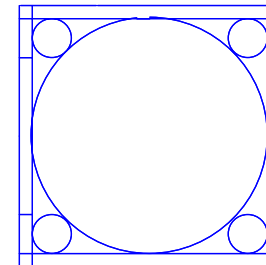


CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

SOCKET_M2

M2_RM[12KRC-04K807-22R_12KRC-04K807-23R]



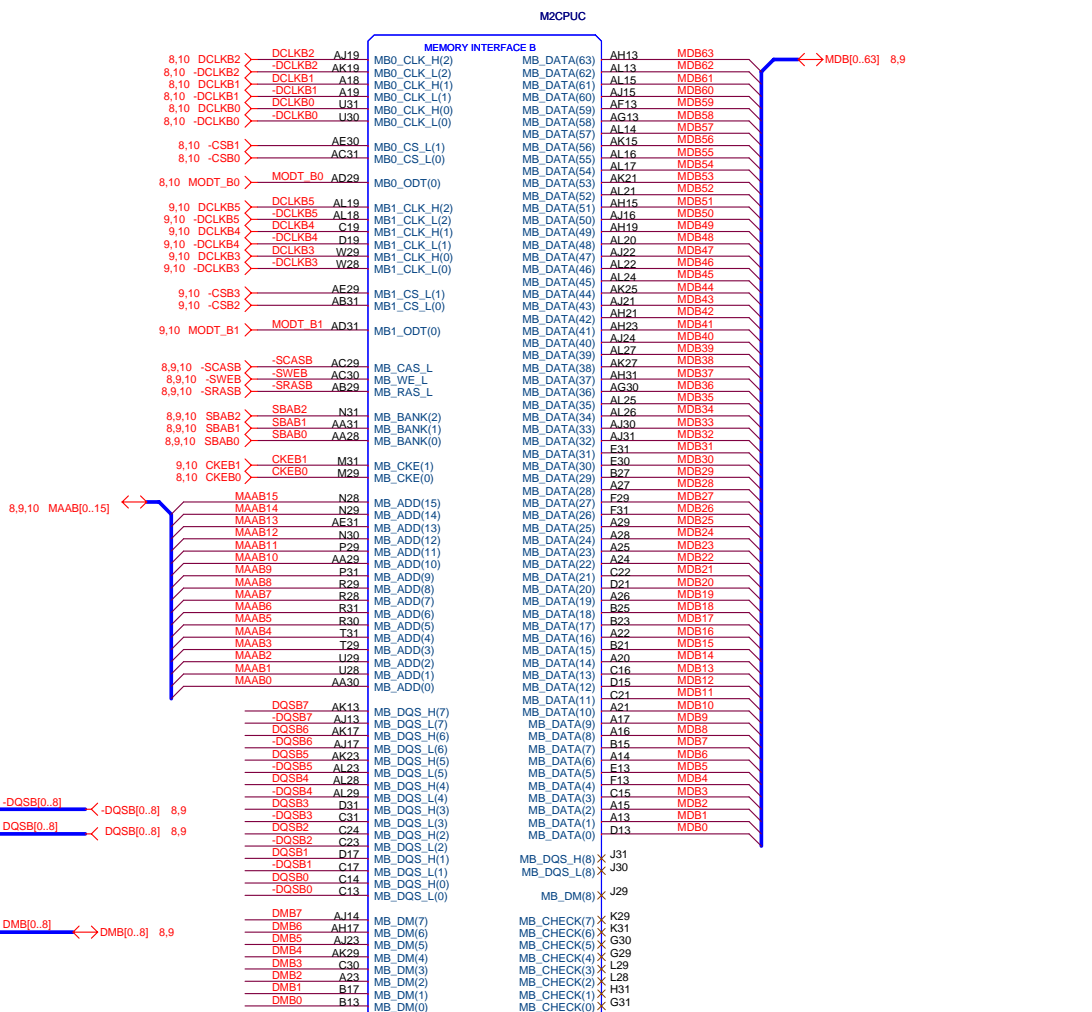
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File
CPU HYPER TRANSPORT

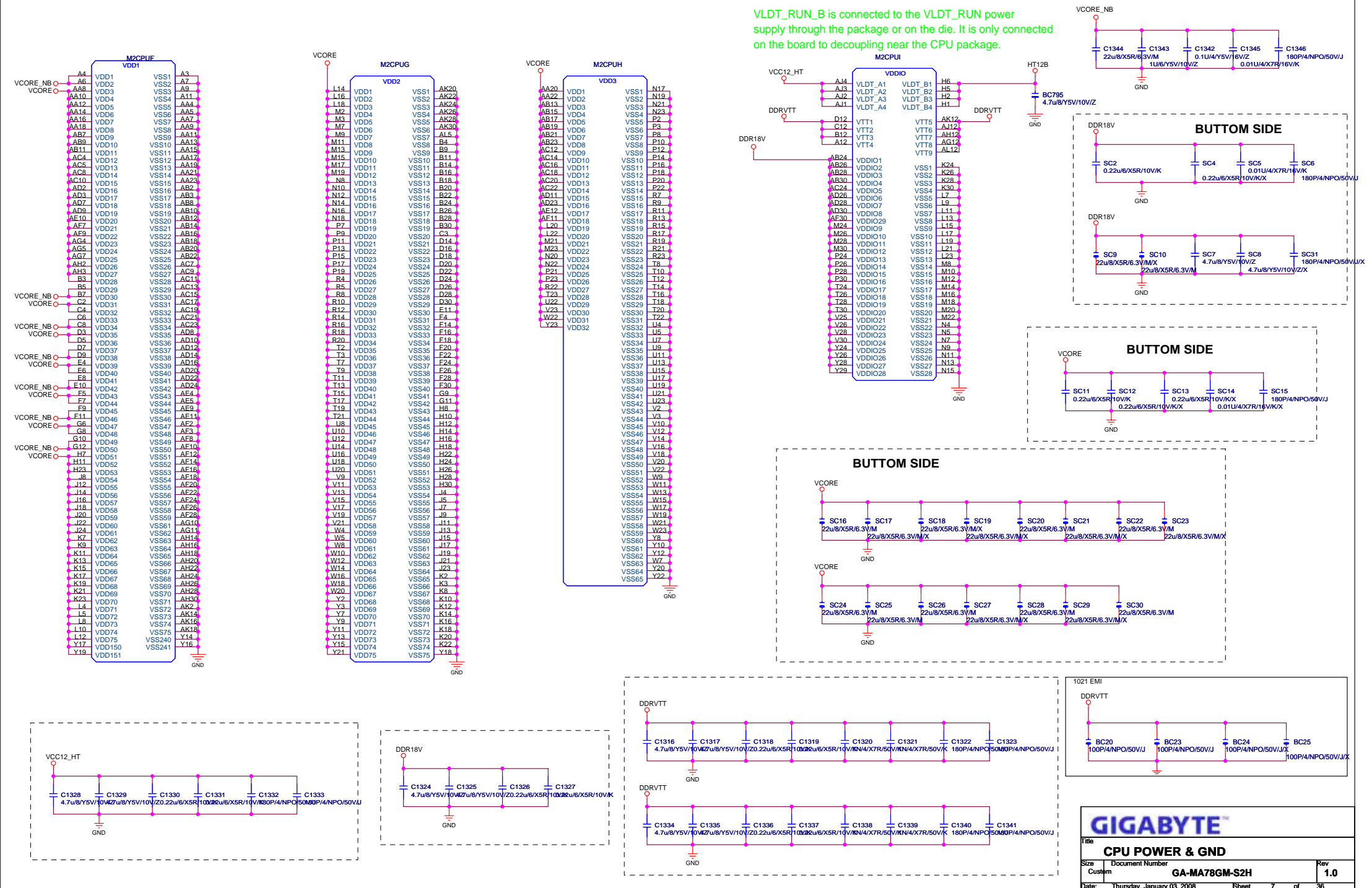
Size Custom Document Number
GA-MA78GM-S2H

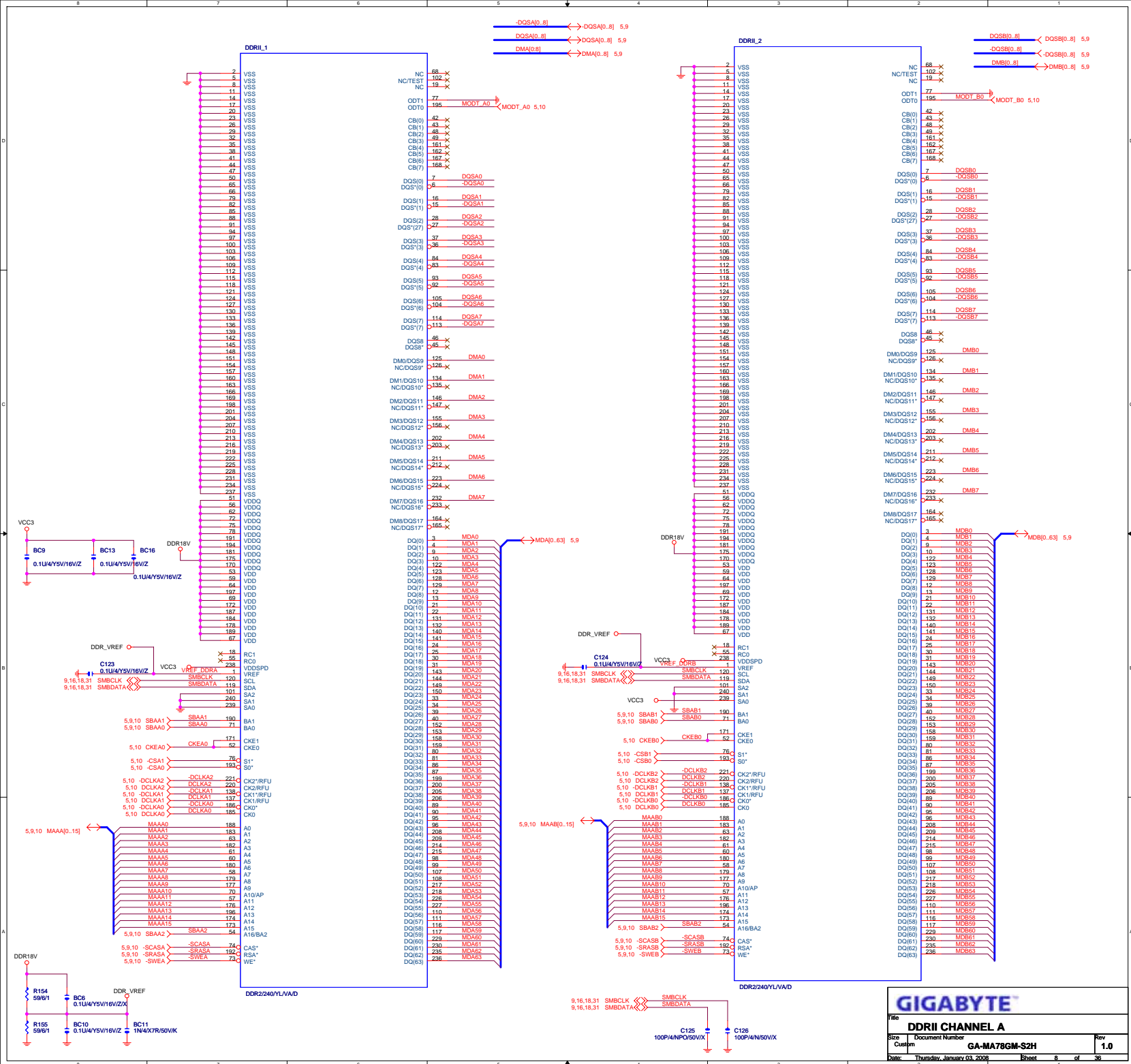
Rev
1.0

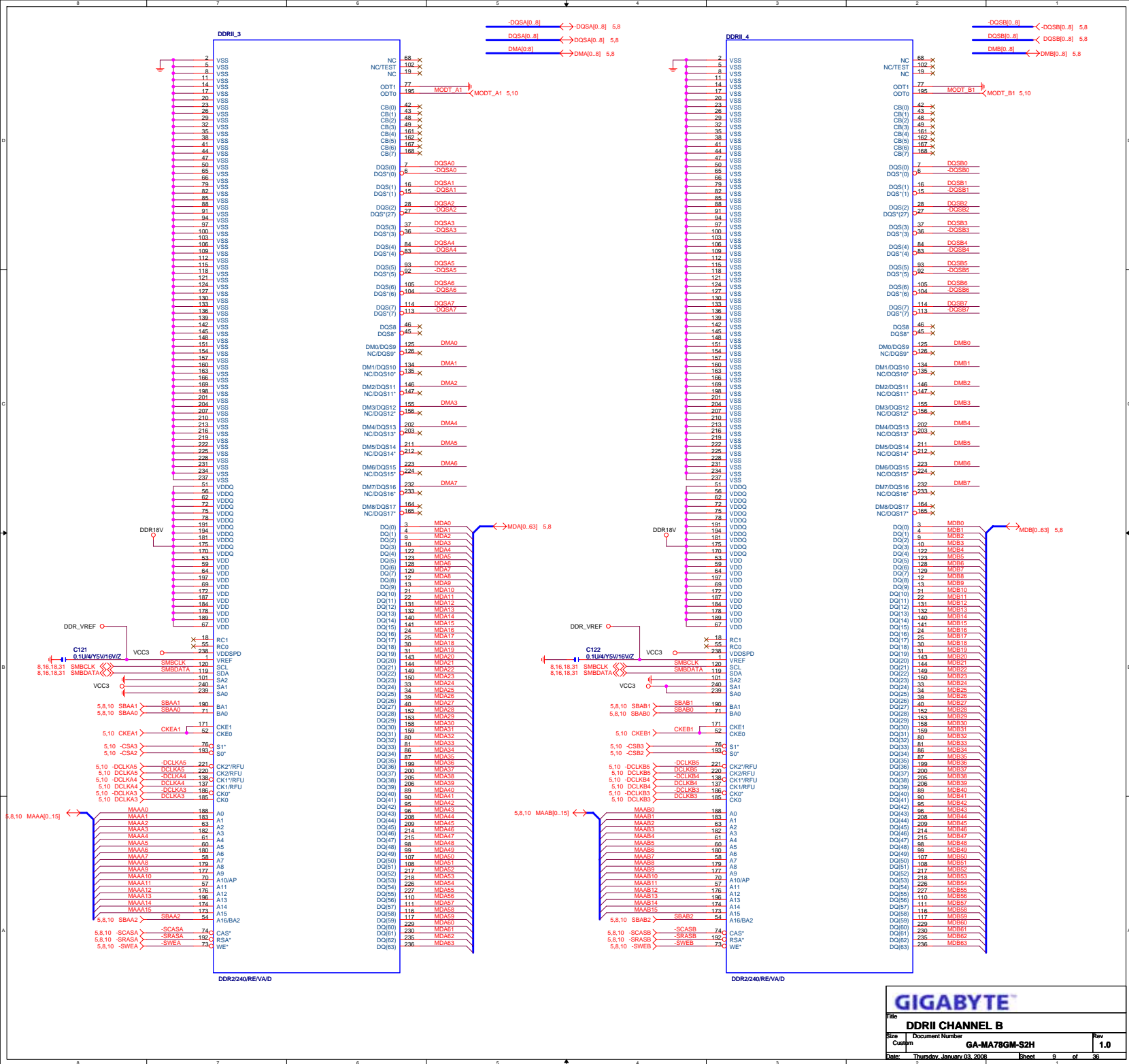
Date: Thursday, January 03, 2008 Sheet 4 of 36

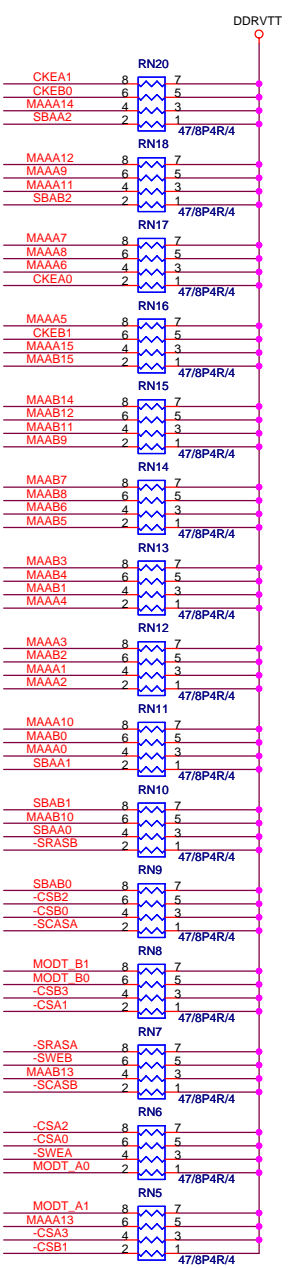
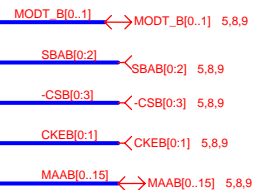
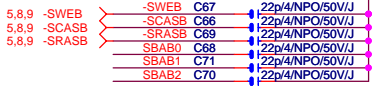
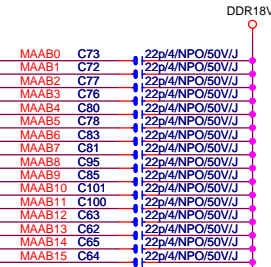
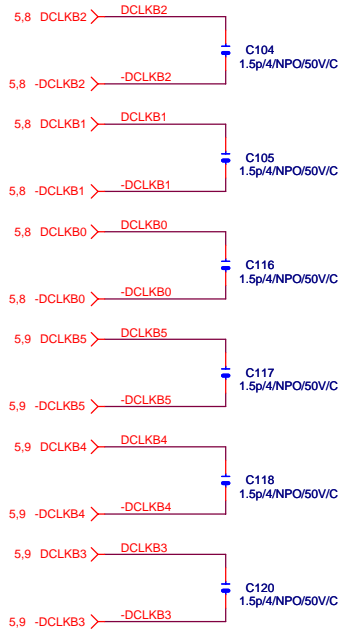
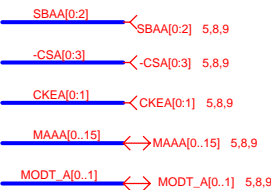
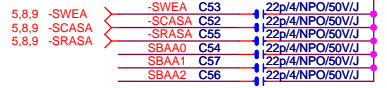
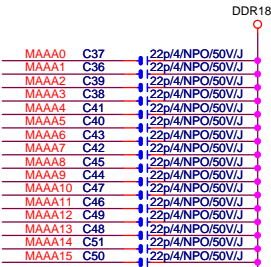
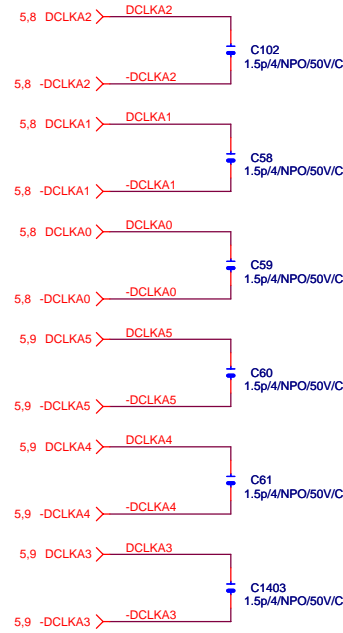
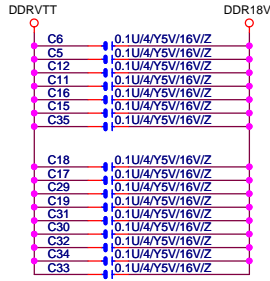
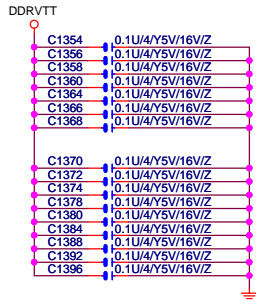


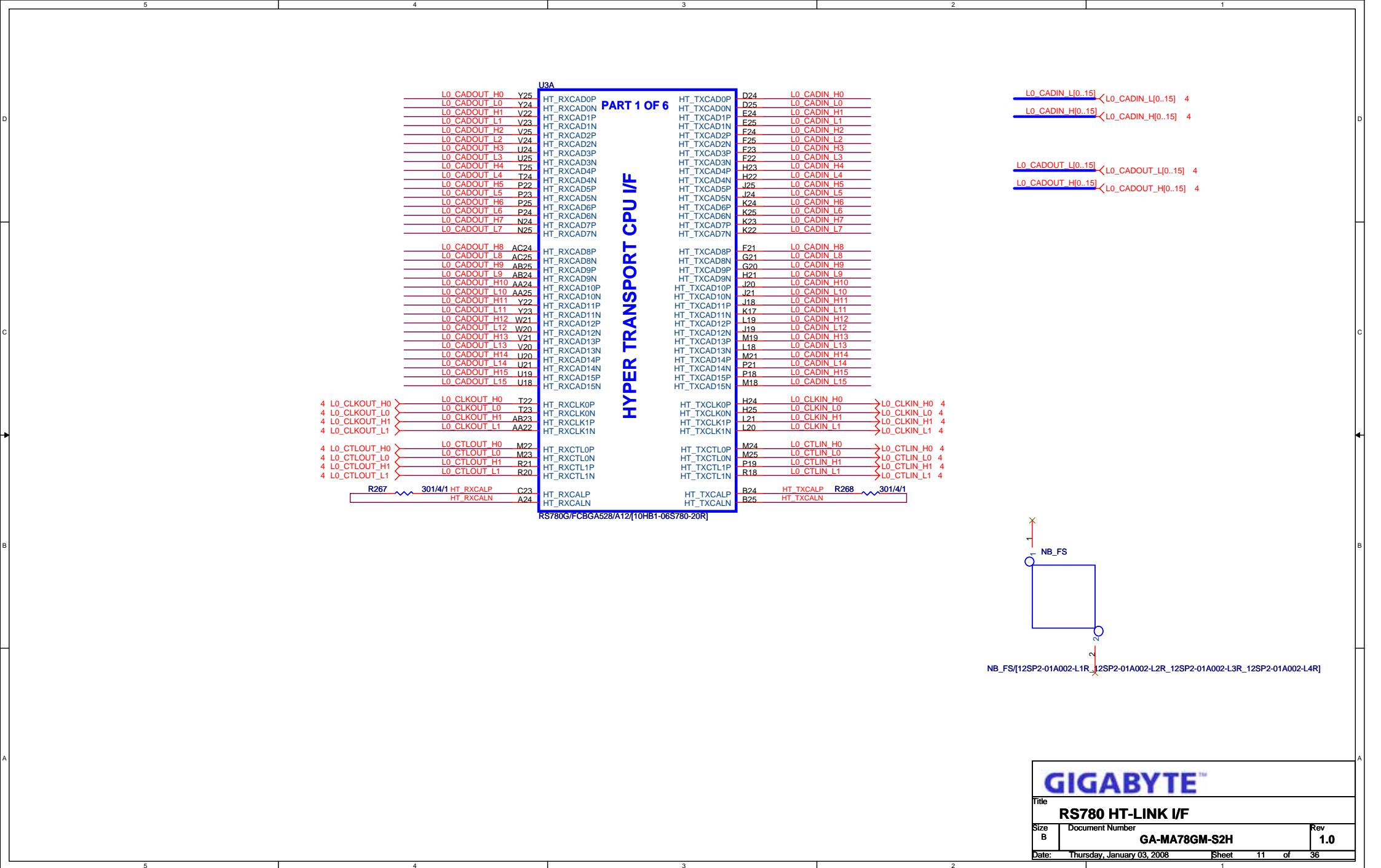
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

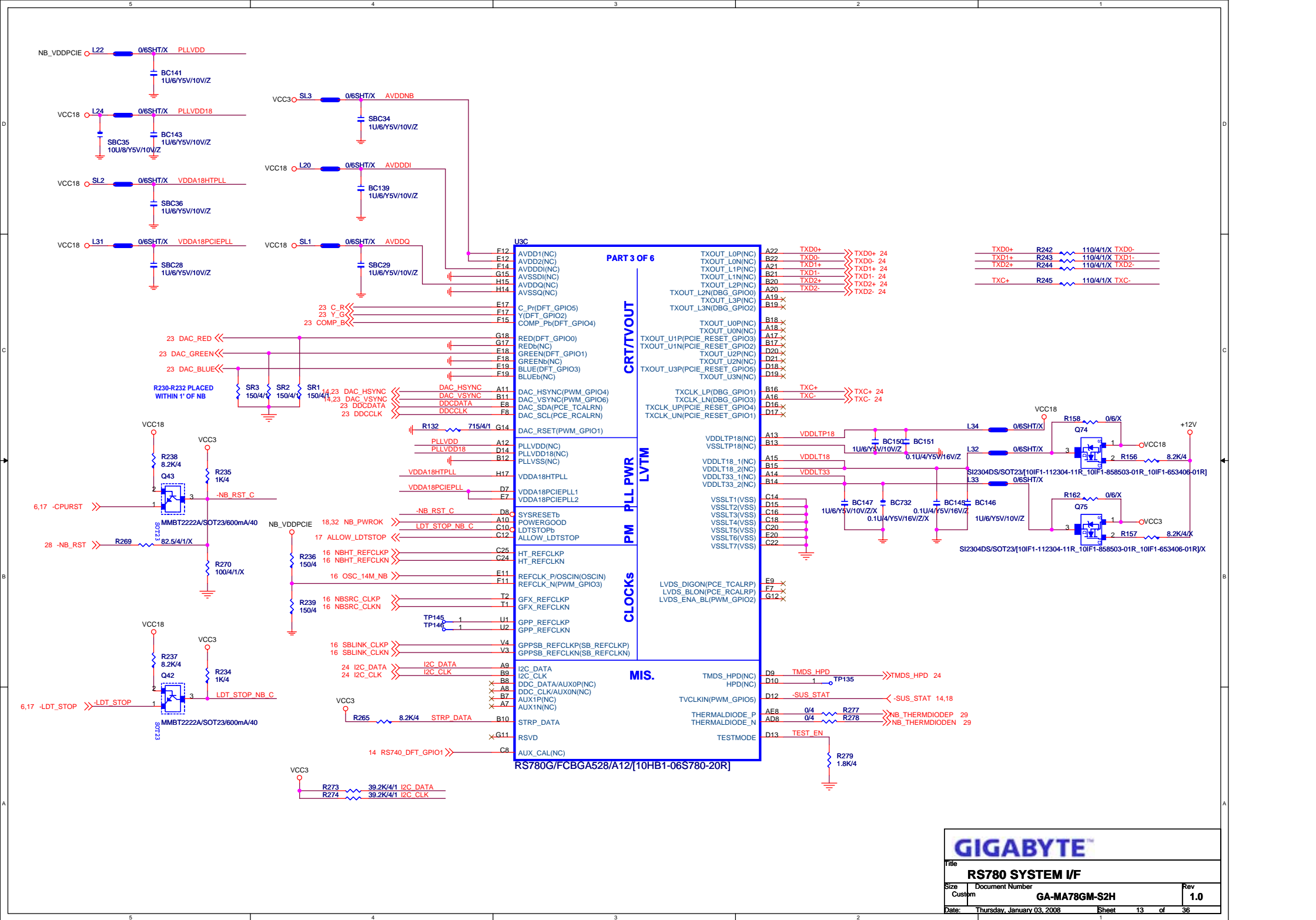


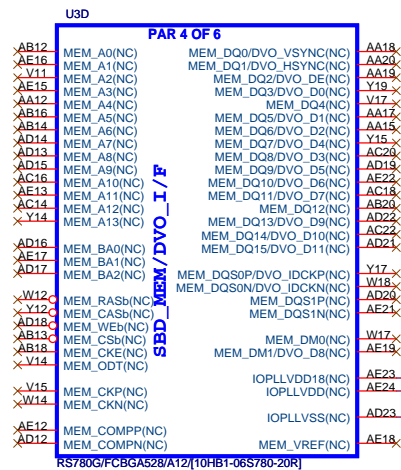












RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

13 RS740_DFT_GPIO1 >>> R272 150/4

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

13.18 -SUS_STAT D5 >>> A_RST 17,25,28

13.23 DAC_VSYNC <<< R276 3K/4 >>> VCC3
R282 10K/4/X

Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

13.23 DAC_HSYNC <<< R286 10K/4/X >>> VCC3
R285 3K/4

Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected

RS740: pin DFT_GPIO1

RX780: pin DFT_GPIO1

RS780: pin SUS_STAT#

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.

111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
000: 4-0-0-0-0 Config F
others: register defined (default to Config E)

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1 Mode L default
1-1-1-1-1-1 Mode L
2-0-2-0-2-0 Mode C2
2-0-2-0-1-1 Mode K
2-0-1-1-1-1 Mode E
1-1-1-1-1-1 Mode L
4-0-0-0-1-1 Mode C
4-0-0-0-2-0 Mode B

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory

1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)

RS740: pin DFT_GPIO0

RS780: pin HSYNC

RX780: Not Applicable

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus

using PCIE bus

1. Disable (can be enabled thru nbcfg register)

0 : Enable

RX780: pin DFT_GPIO0

RS780: configurable thru register

setting only

RS740: Not supported

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Title

RS780 STRAP

Size

Document Number

GA-MA78GM-S2H

Rev

1.0

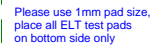
Date: Thursday, January 03, 2008

Sheet

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36

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLT18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



RS780 POWER & GND

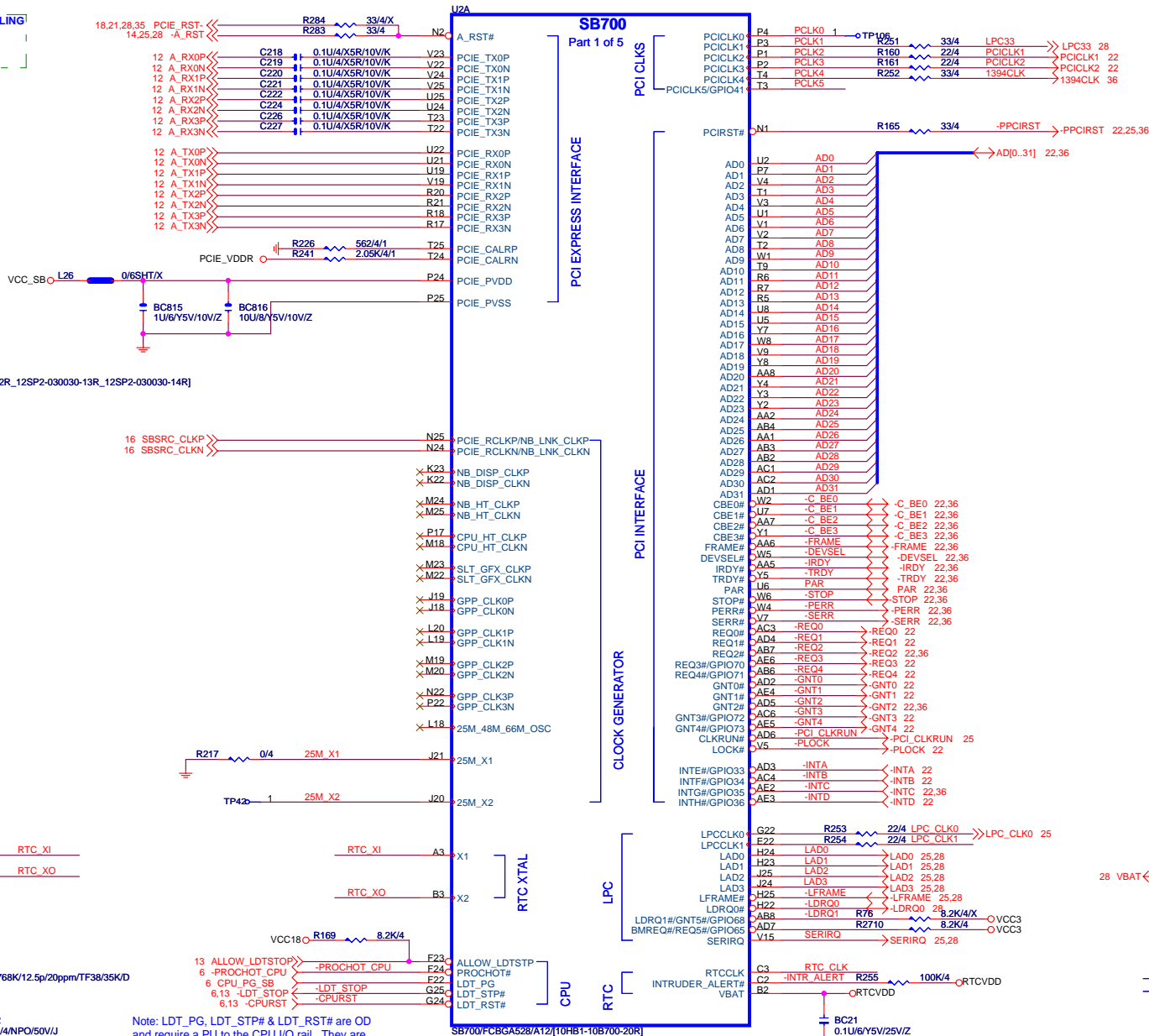
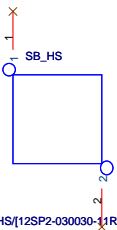
GA-MA78GM-S2H

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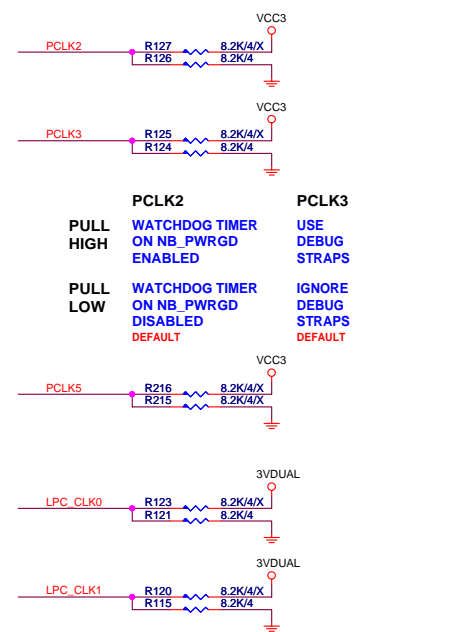


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK



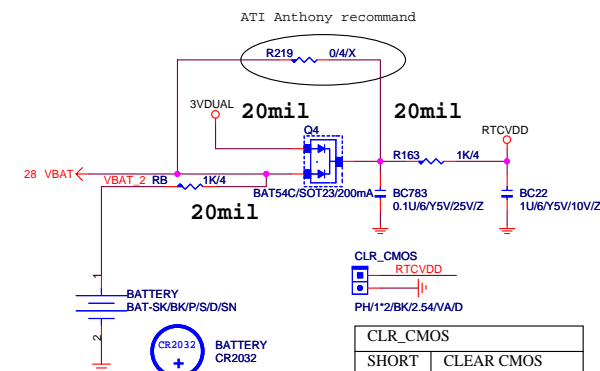
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



LPC_CLK0 LPC_CLK1

PULL HIGH WATCHDOG TIMER ON NB_PWRGD ENABLED
PULL LOW WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT

USE DEBUG STRAPS
IGNORE DEBUG STRAPS DEFAULT

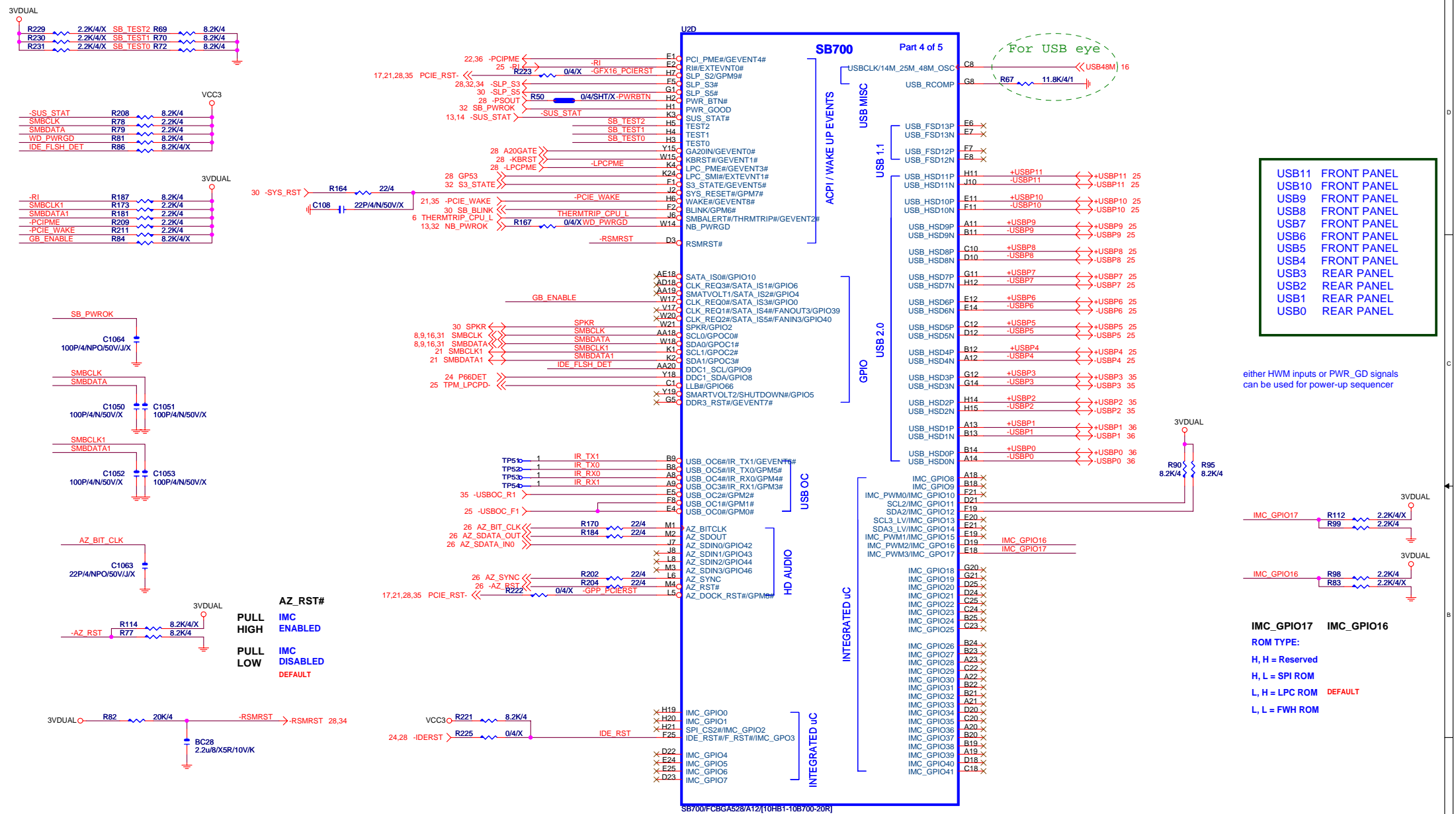


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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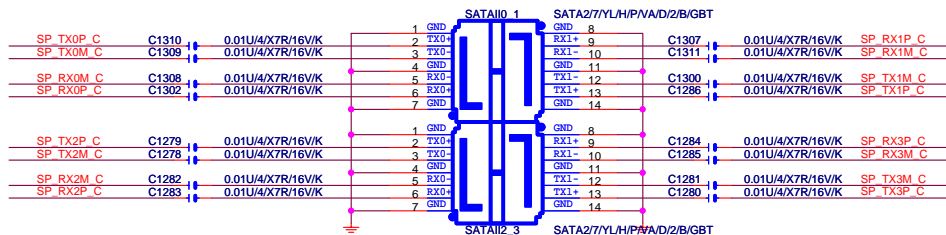
ATI SB700 PCIE/PCI/CPU/LPC		
Size Custom	Document Number GA-MA78GM-S2H	Rev 1.0
Date: Thursday, January 03, 2008	Sheet 17	of 36



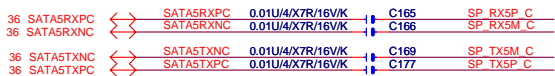
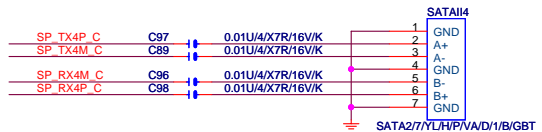
USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM
L, H = LPC ROM DEFAULT
L, L = FWH ROM

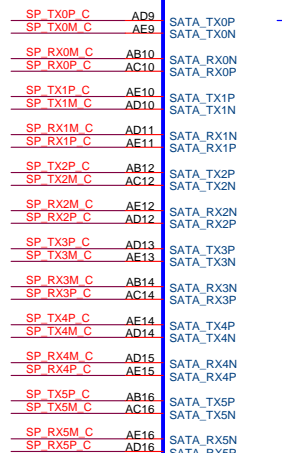
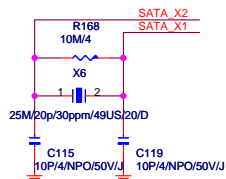
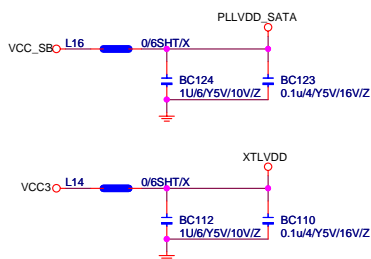


PLACE SATA AC COUPLING
CAPS CLOSE TO SB600



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:
 R650 IS 1K 1% FOR 25MHz
 XTAL, 4.99K 1% FOR 100MHz
 INTERNAL CLOCK



SERIAL ATA

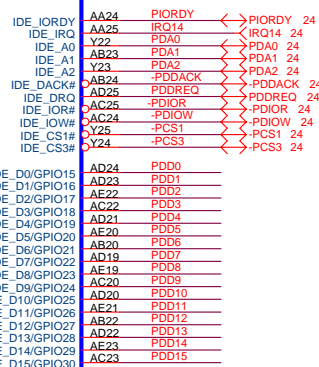
SATA PWR

HW MONITOR

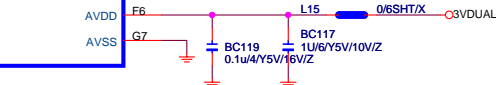
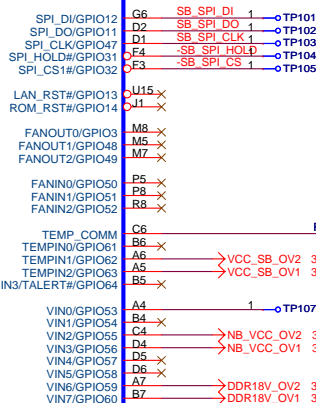
ATA 66/100/133

SPI ROM

HW MONITOR



PDD0[0.15] ↔ PDD0[0.15] 24



SB700/FC6GA520/A12/[10H81-10B700-20R]

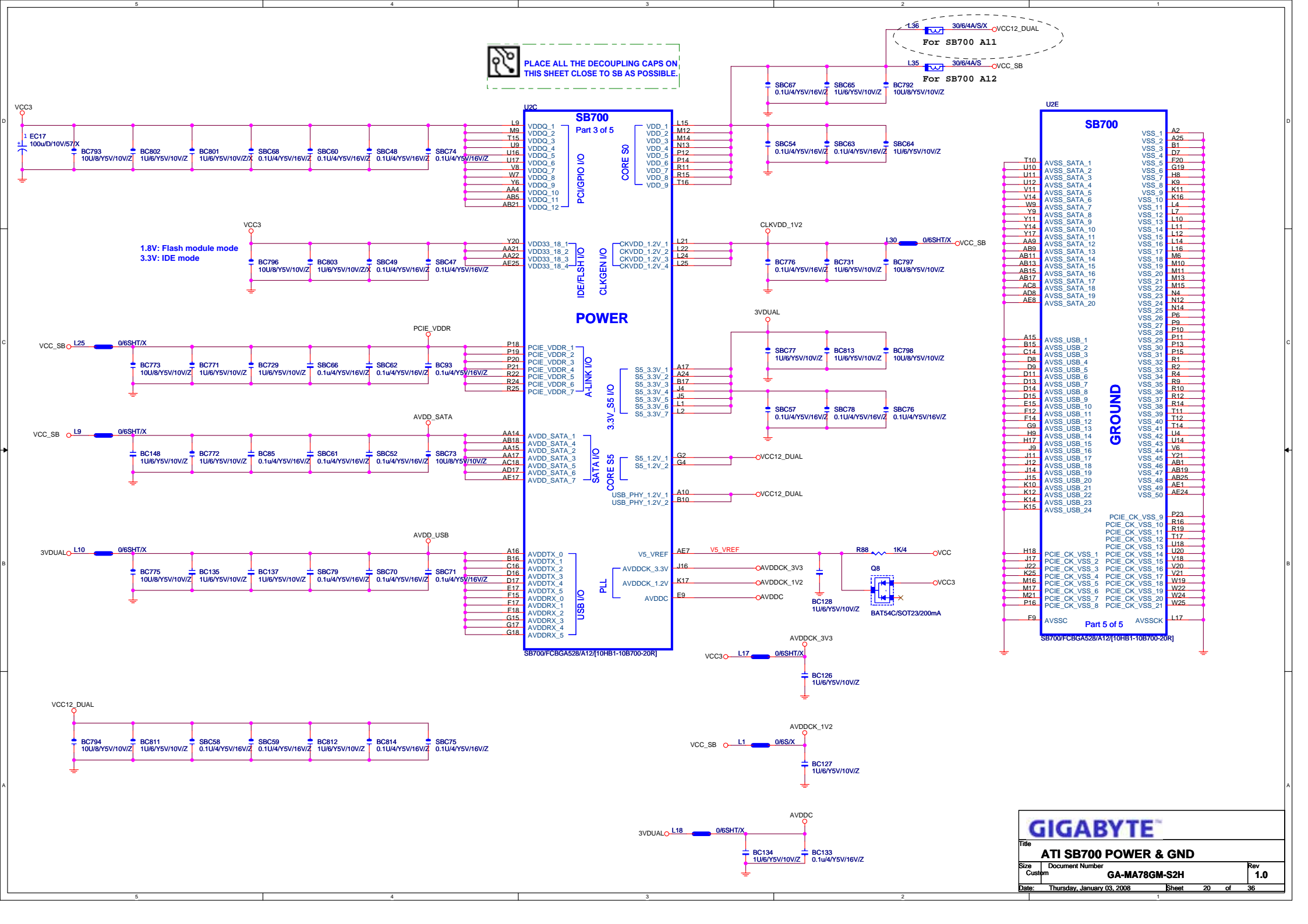
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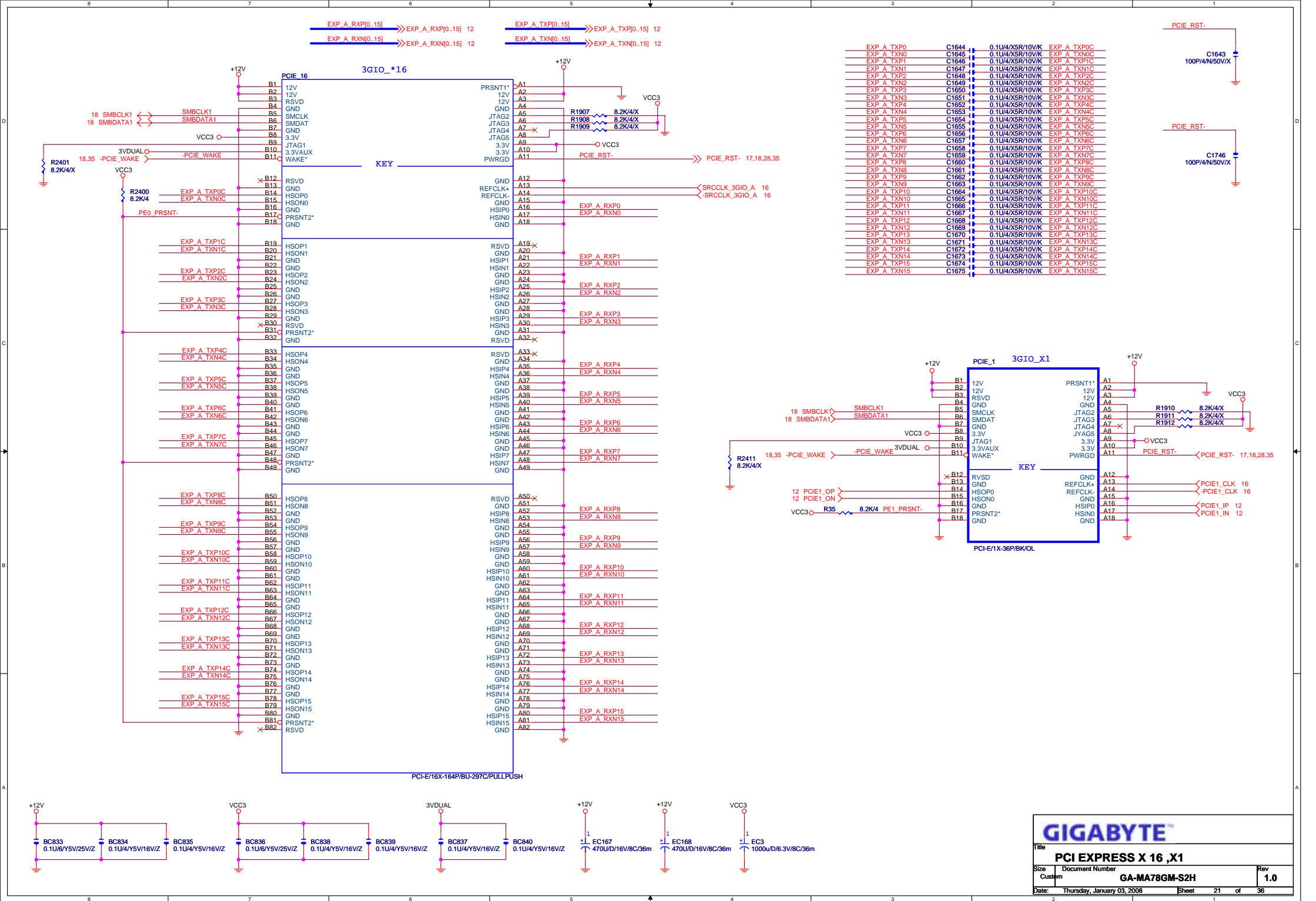
ATI SB700 SATA/IDE/HWM/SPI

Size Custom Document Number GA-MA78GM-S2H Rev 1.0
 Date: Thursday, January 03, 2008 Sheet 19 of 36



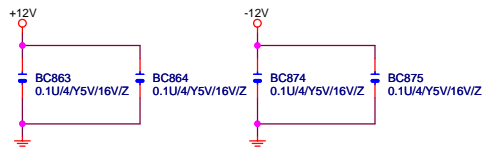
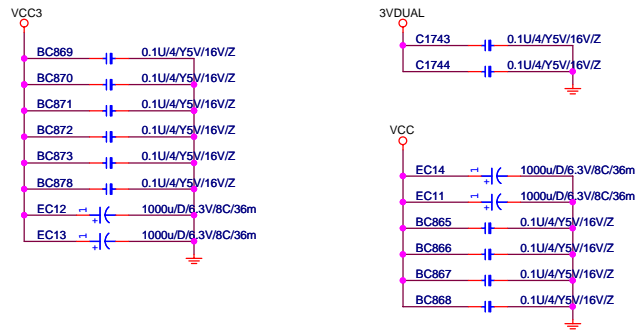
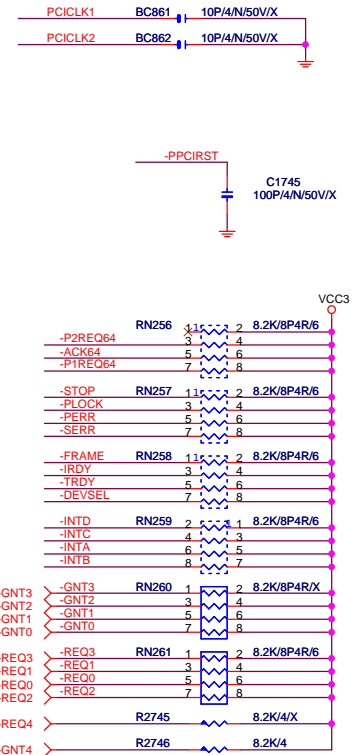
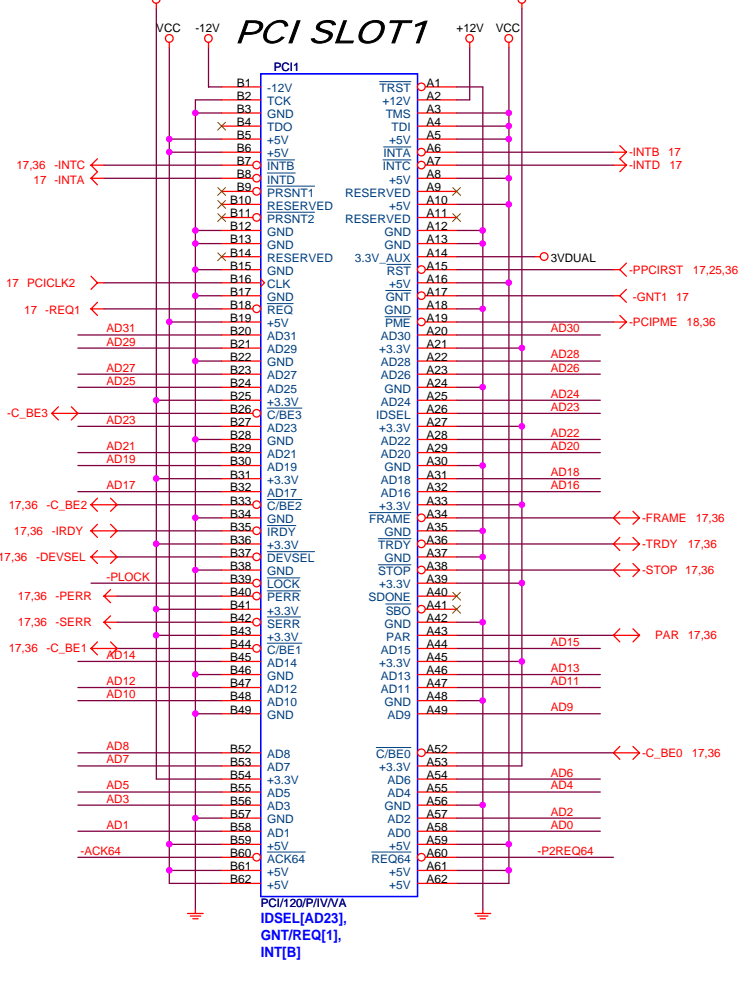
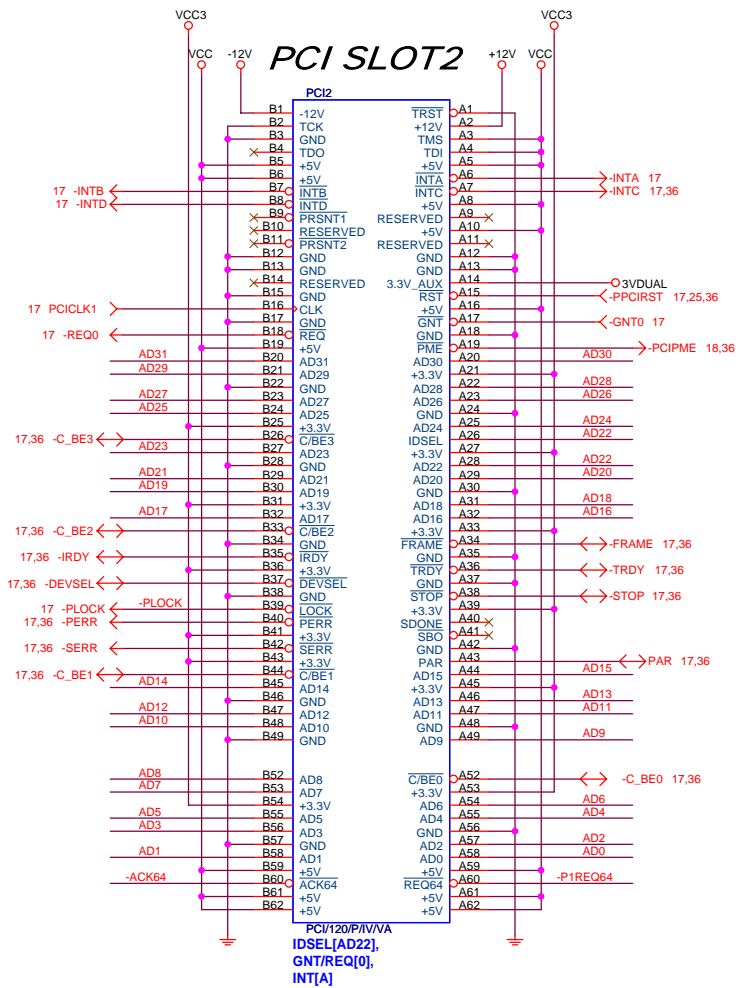
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.





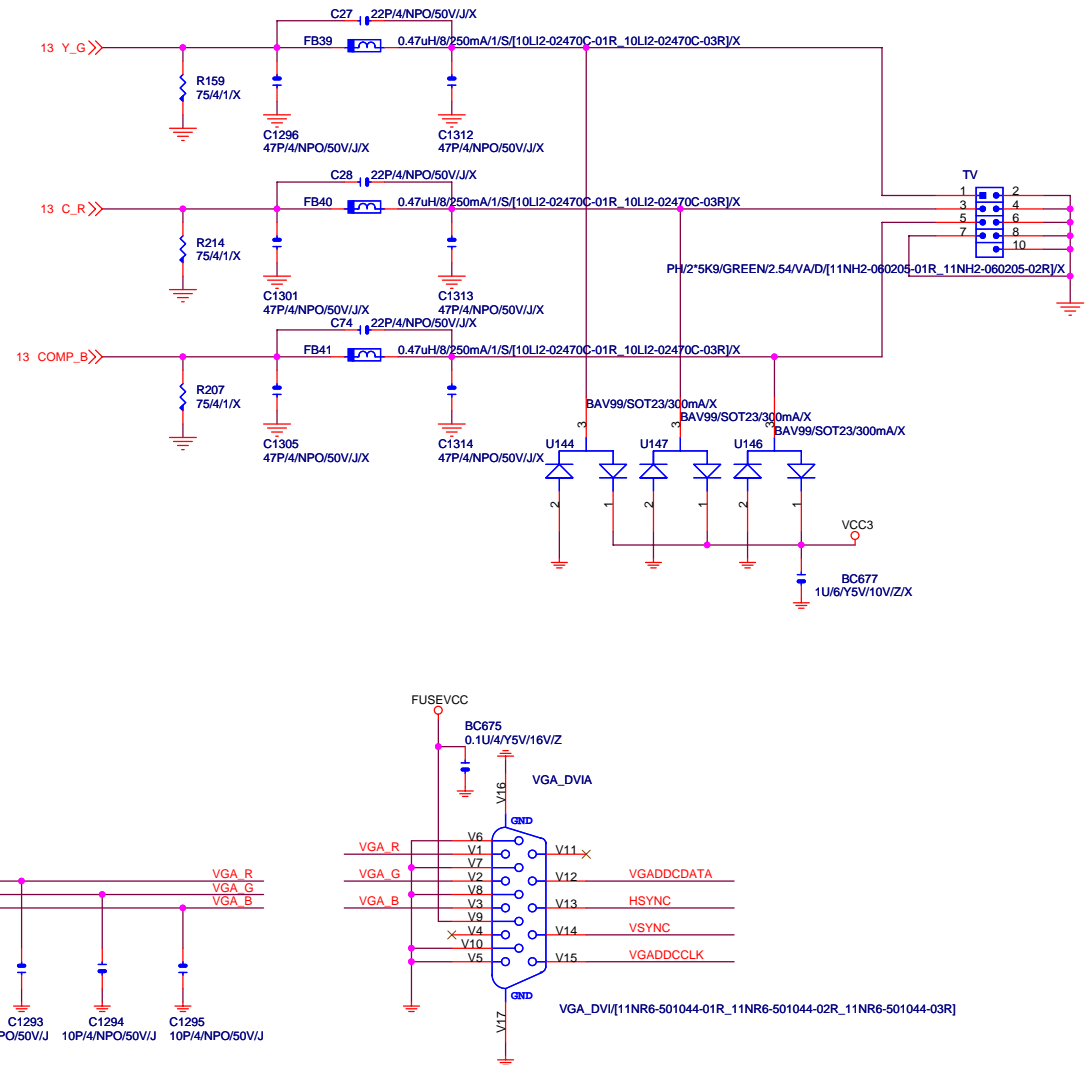
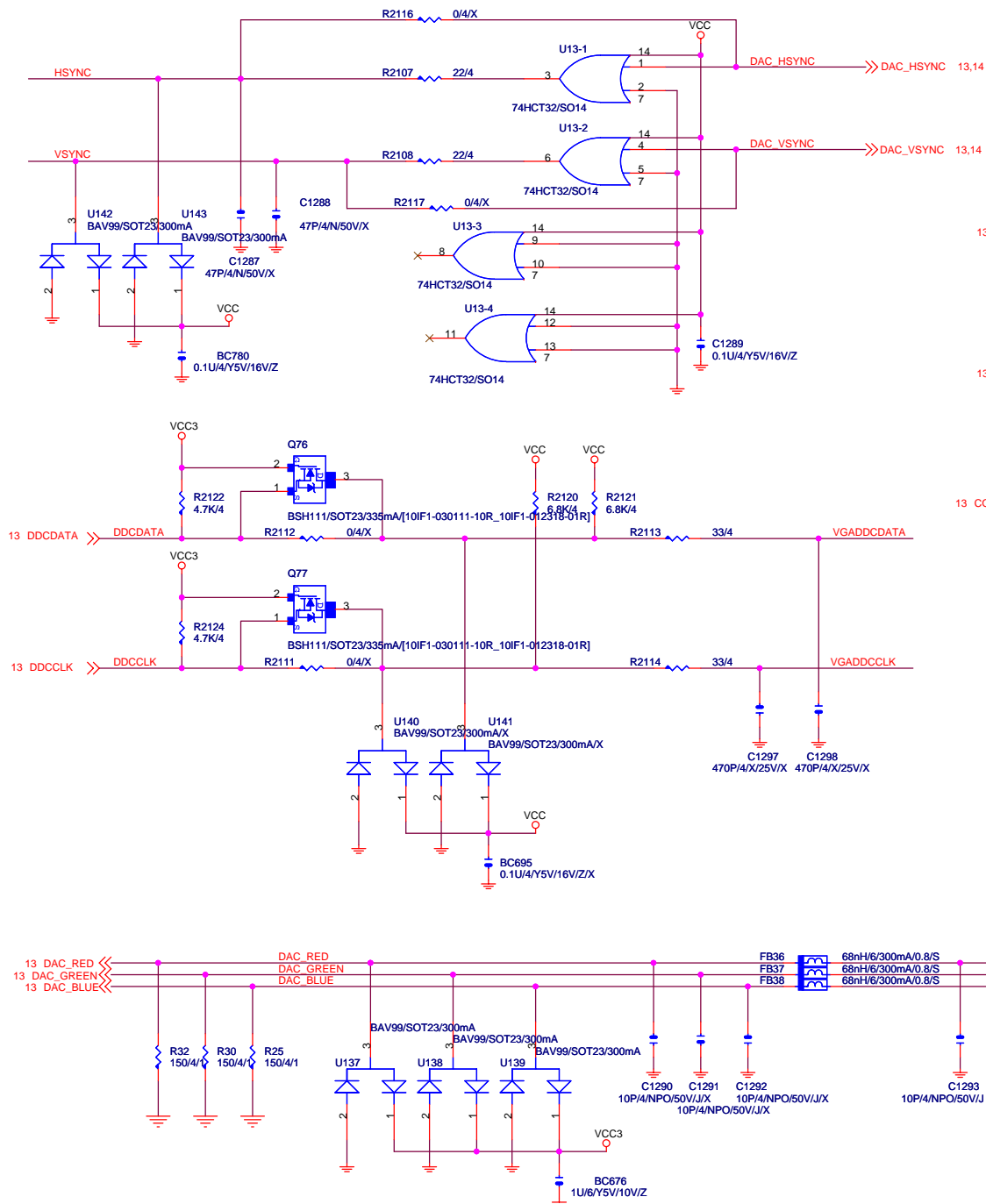
PCI SLOT 1,2

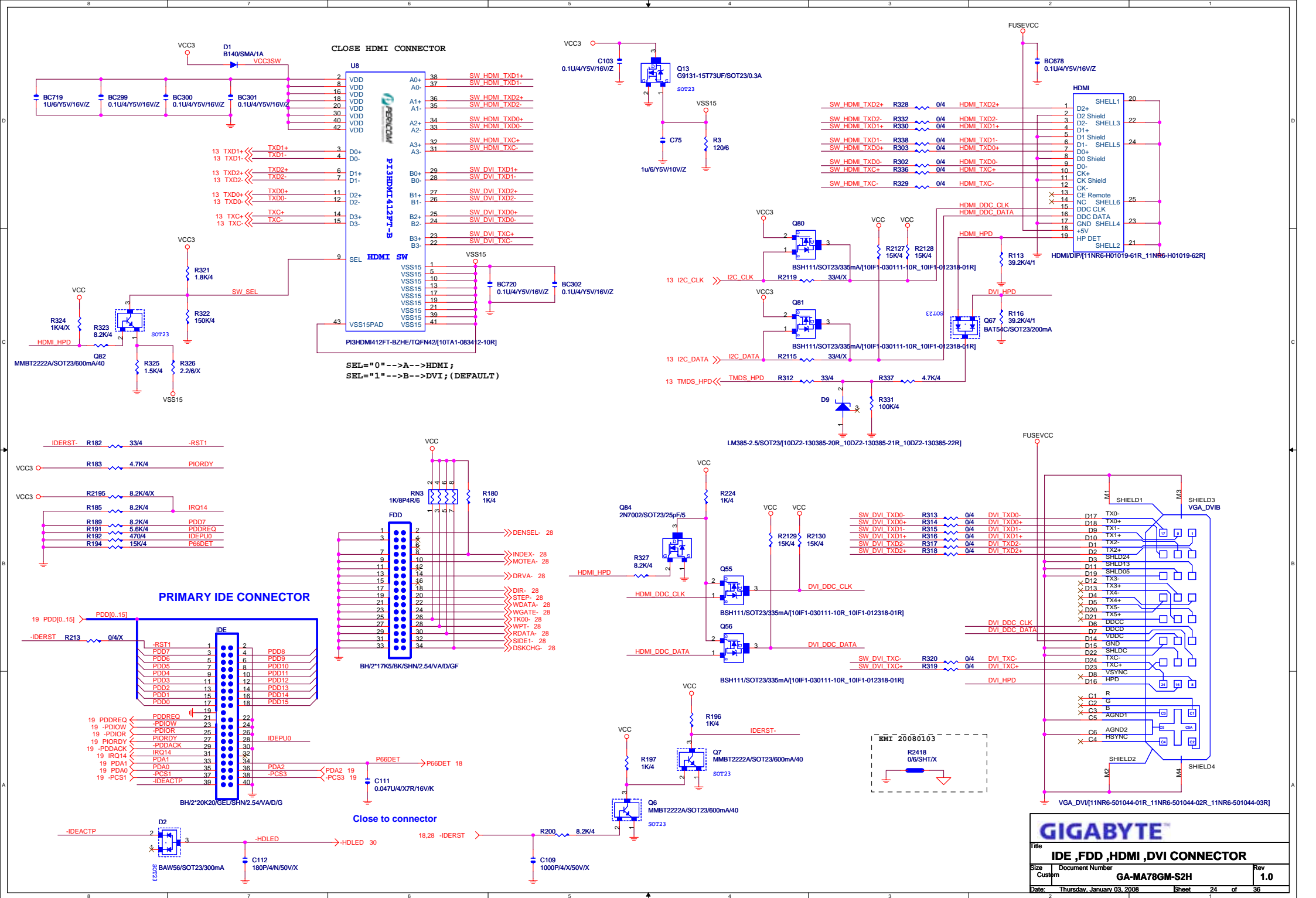
17,36 AD[0..31] ↔ AD[0..31]

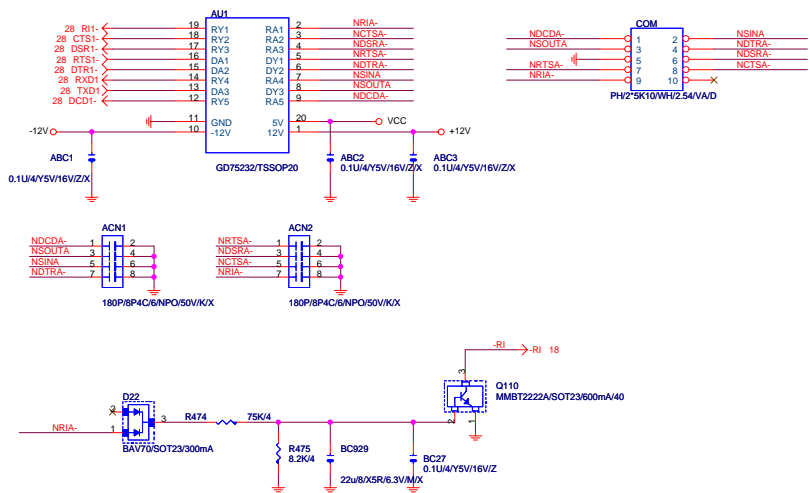


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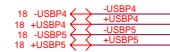
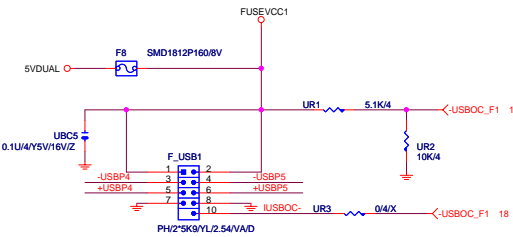
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Size	Document Number	Rev	
Custom	GA-MA78GM-S2H	1.0	
Date:	Thursday, January 03, 2008	Sheet	22 of 36



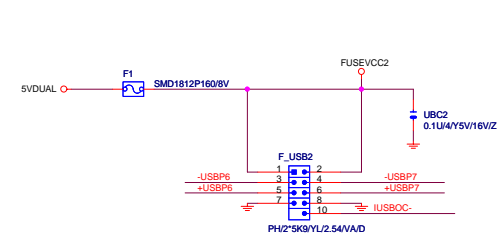




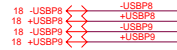
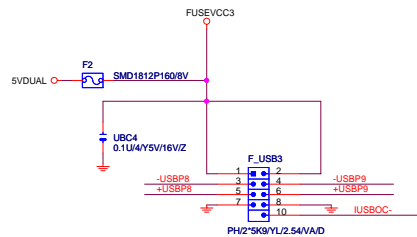
FRONT SIDE USB1



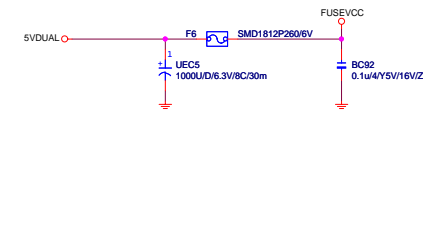
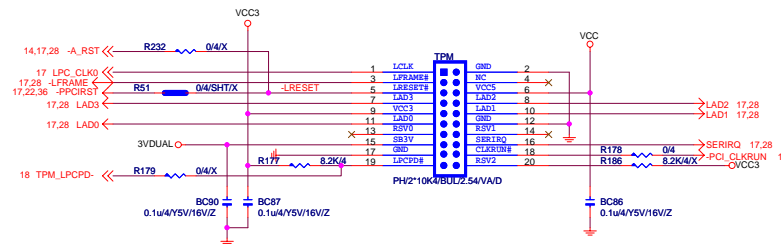
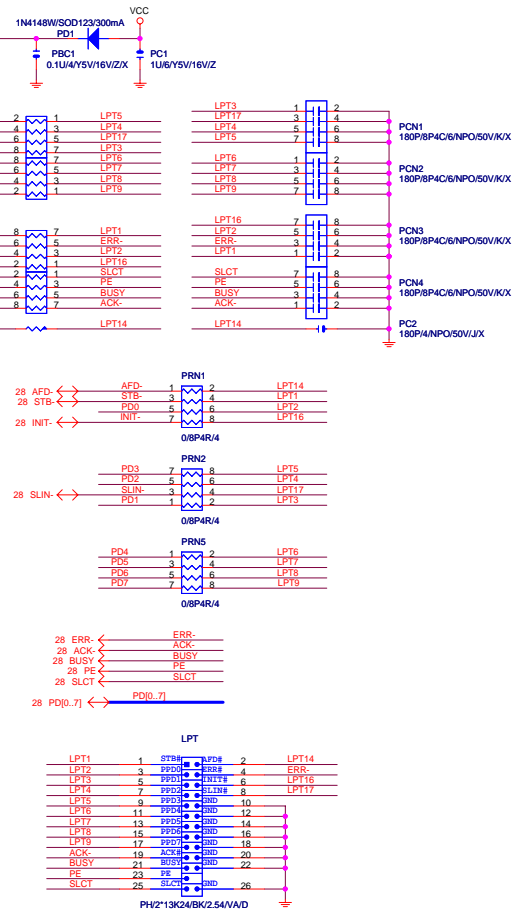
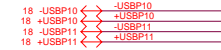
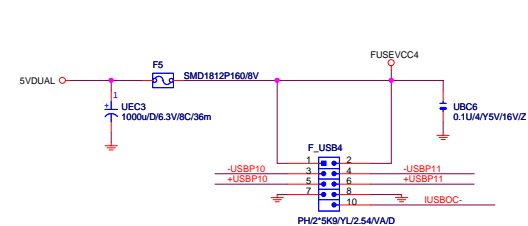
FRONT SIDE USB2



FRONT SIDE USB3

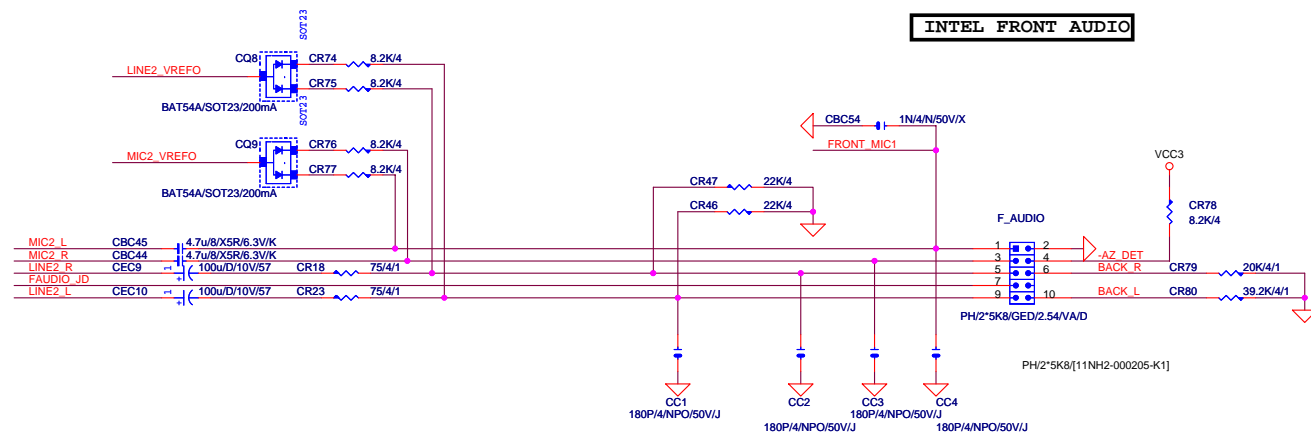
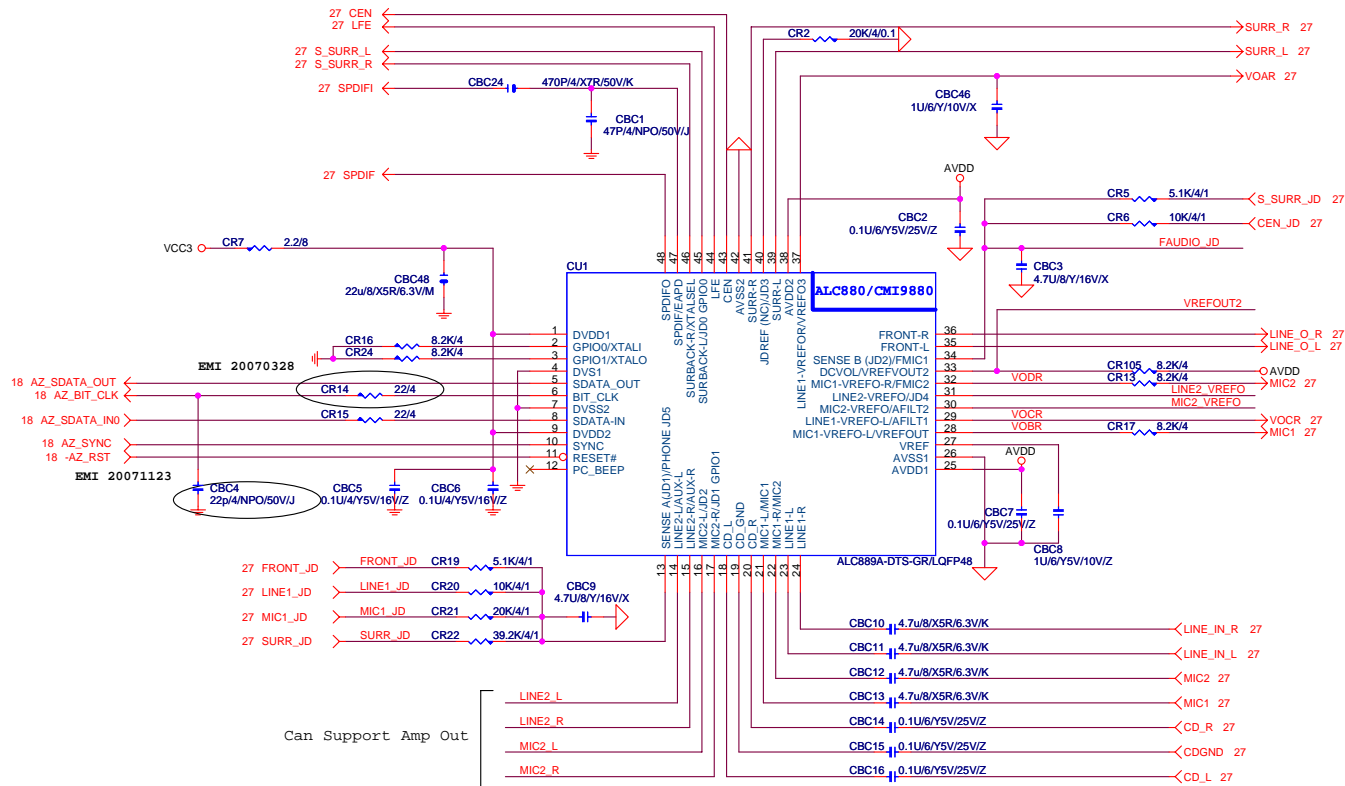


FRONT SIDE USB4

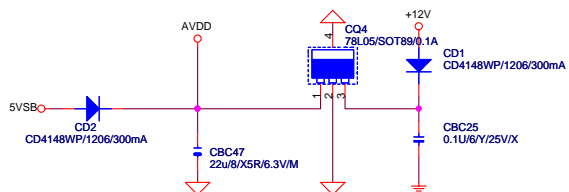
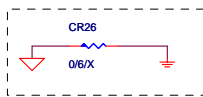


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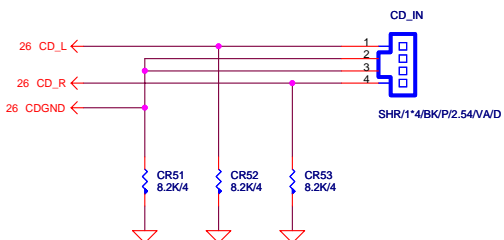
COM/LPT/F_USB/TPM		
Size C	Document Number	Rev
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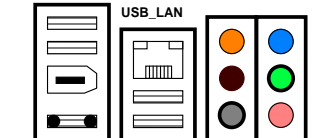
GIGABYTE®			
Title			
ALC889A CODEC			
Size	Document Number	Rev	
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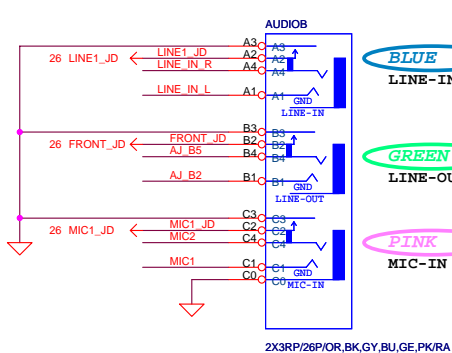
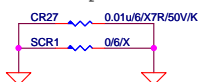
CD IN



USB_1394_ESATA



For Audio precision test



BLUE
LINE-IN

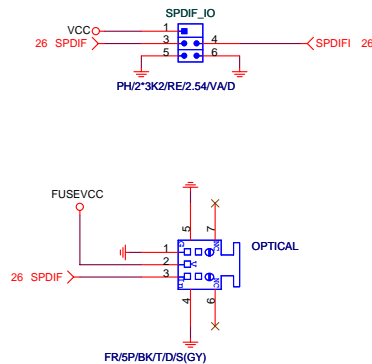
GREEN
LINE-OUT

PINK
MIC-IN

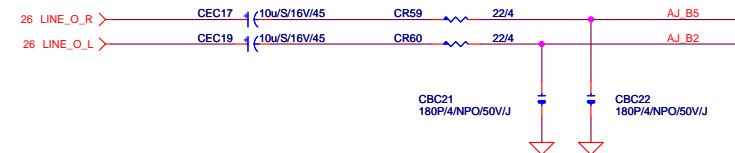
2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R7+15P/[11NR6-403004-11]

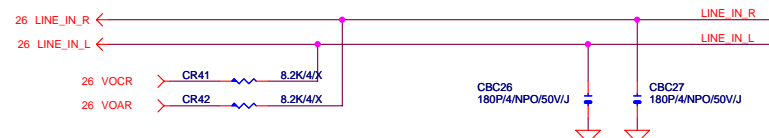
SPDIF



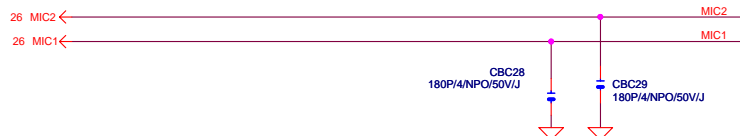
LINE OUT FRONT OUT



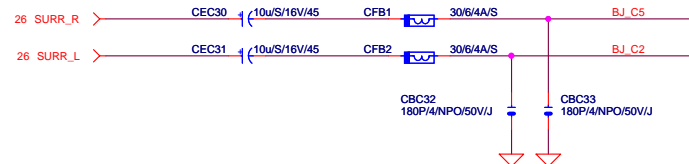
LINE-IN



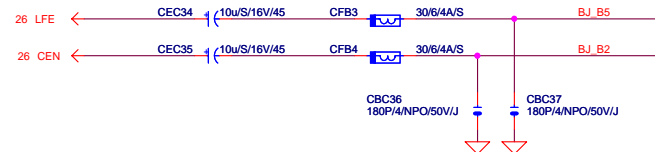
MIC



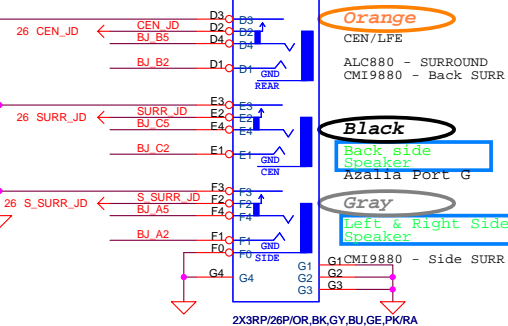
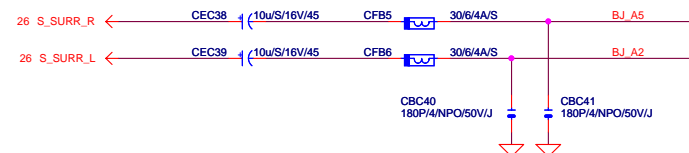
SURROUND



CEN/LFE



SURR BACK



Orange
CEN/LFE
ALC880 - SURROUND
CMI9880 - Back SURR

Black
Back side
Speaker
Azalia Port G

Gray
Left & Right Side
Speaker

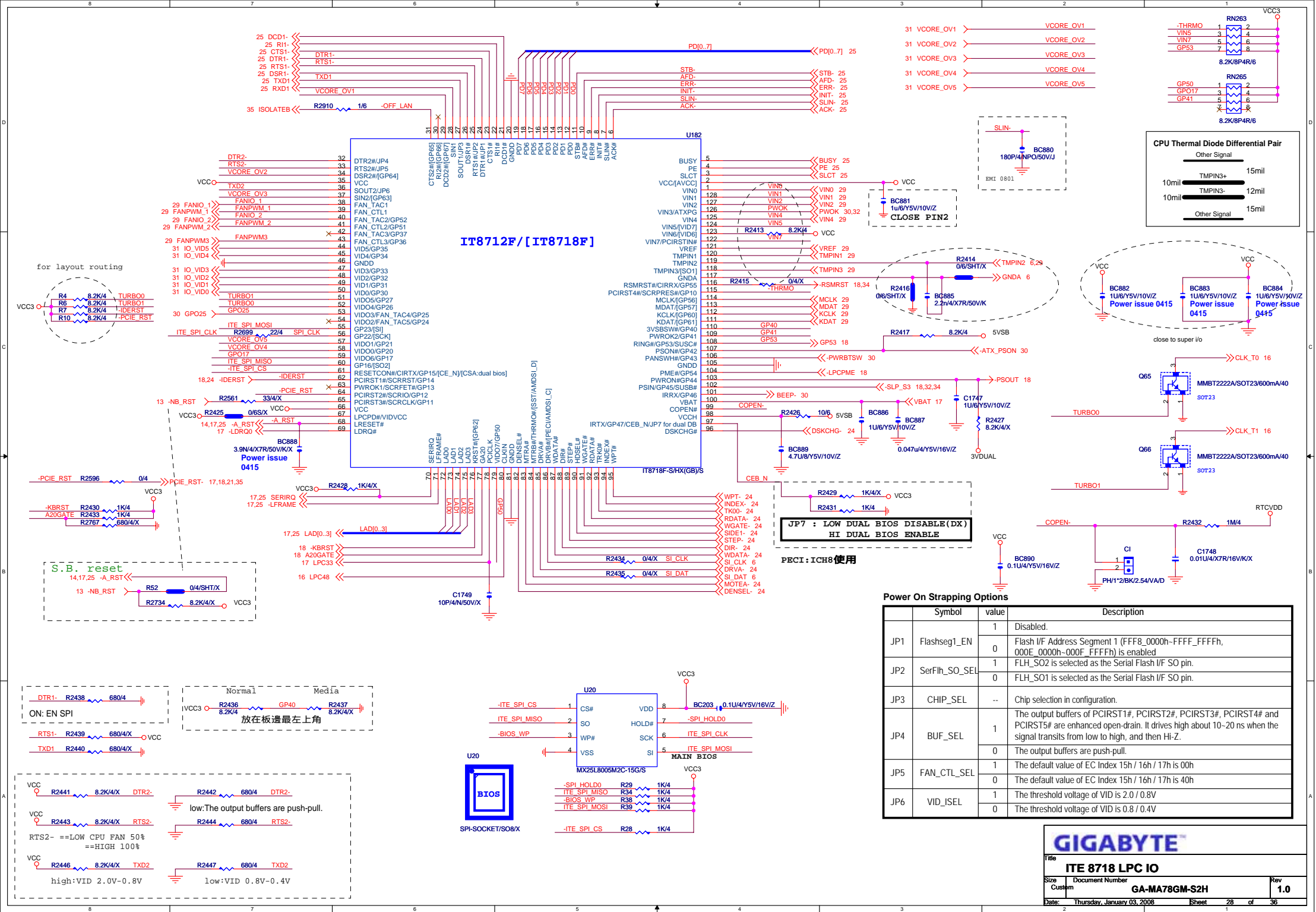
CMI9880 - Side SURR

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

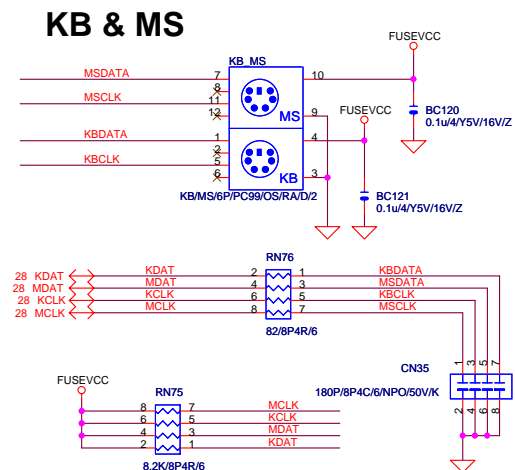
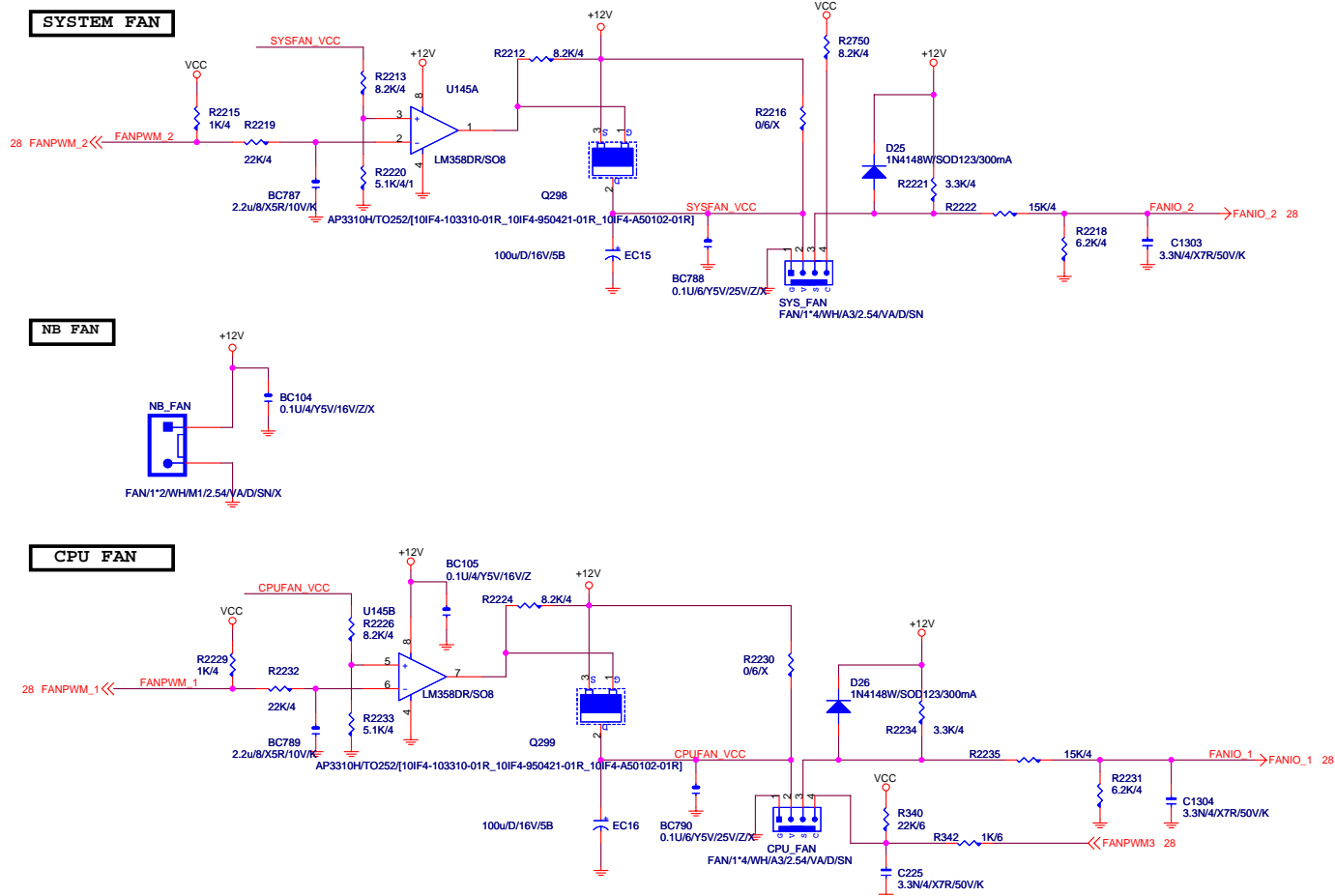
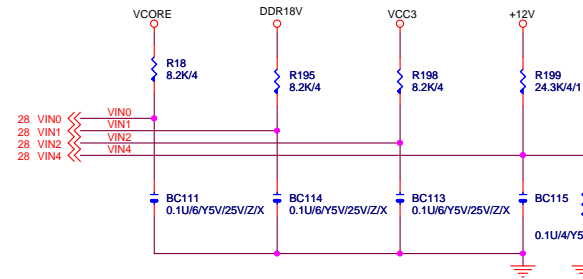
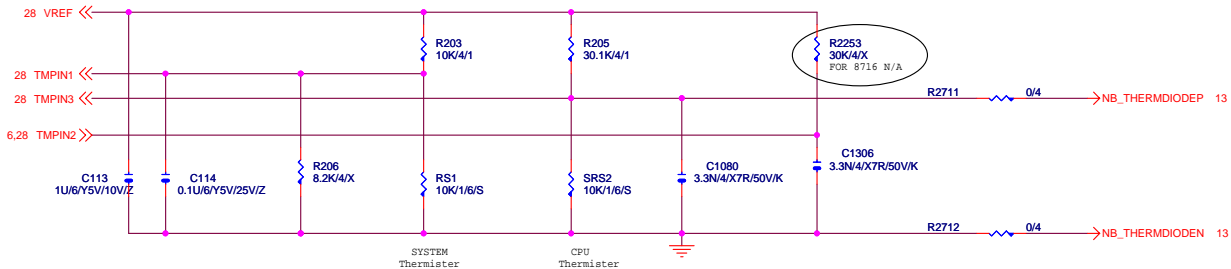
A3R7/13P/ORG/[11NR6-403006-71]
3R7+15P/[11NR6-403004-31]

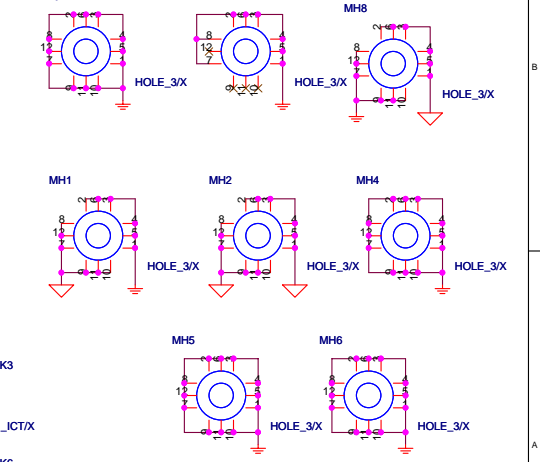
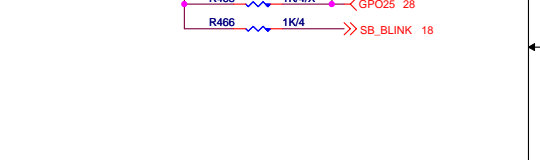
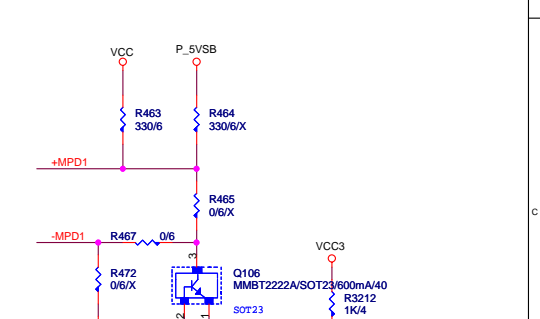
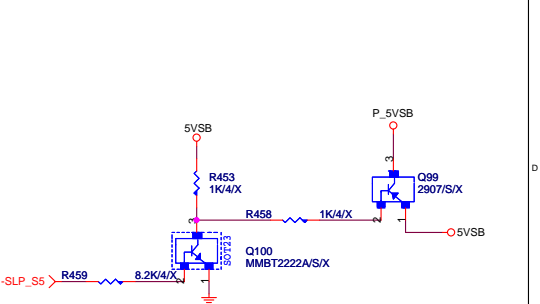
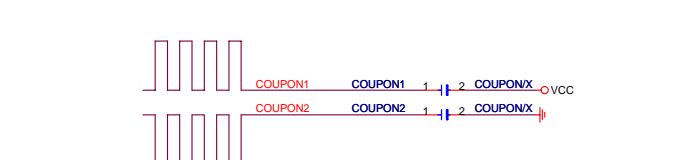
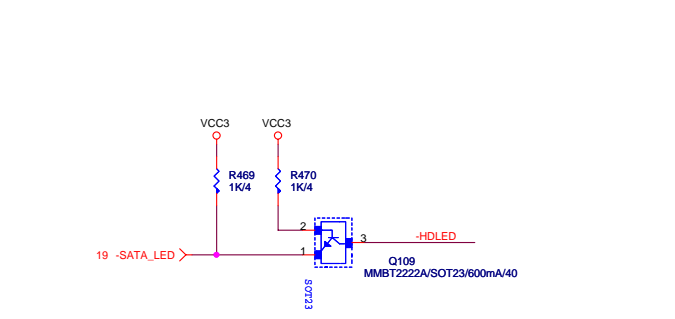
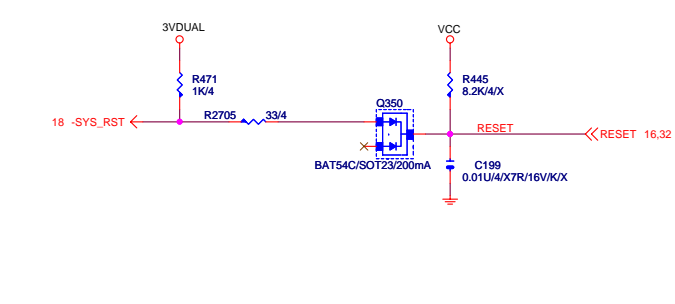
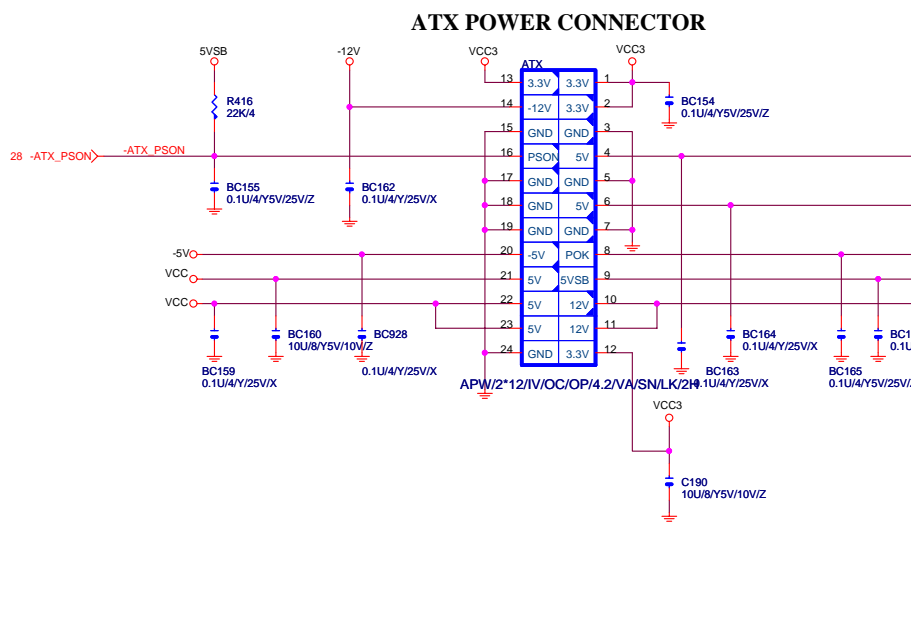
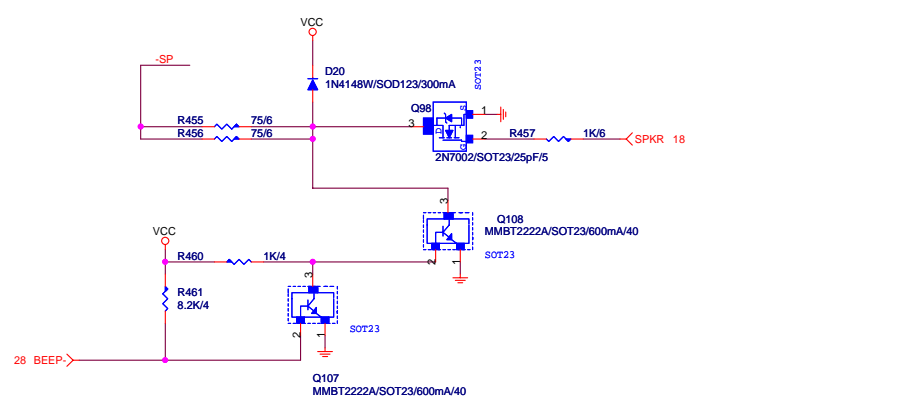
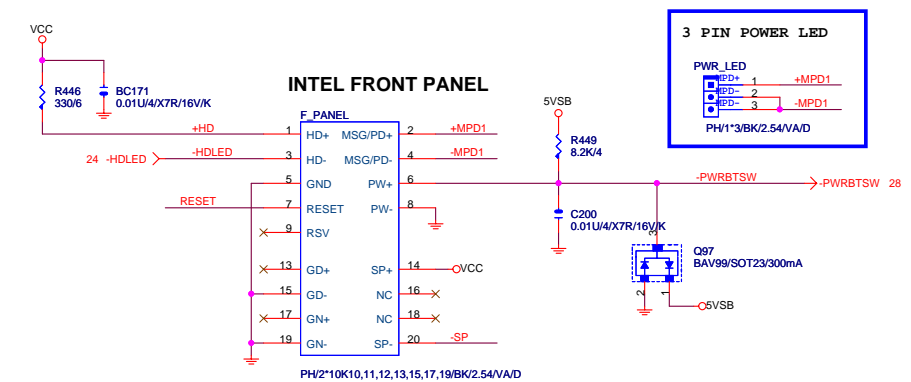
GIGABYTE

Title	AUDIO JACK		
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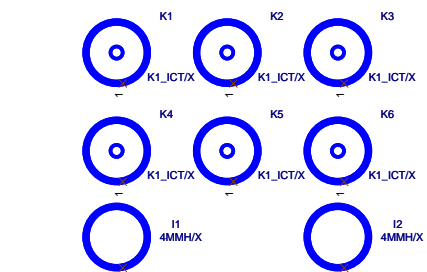


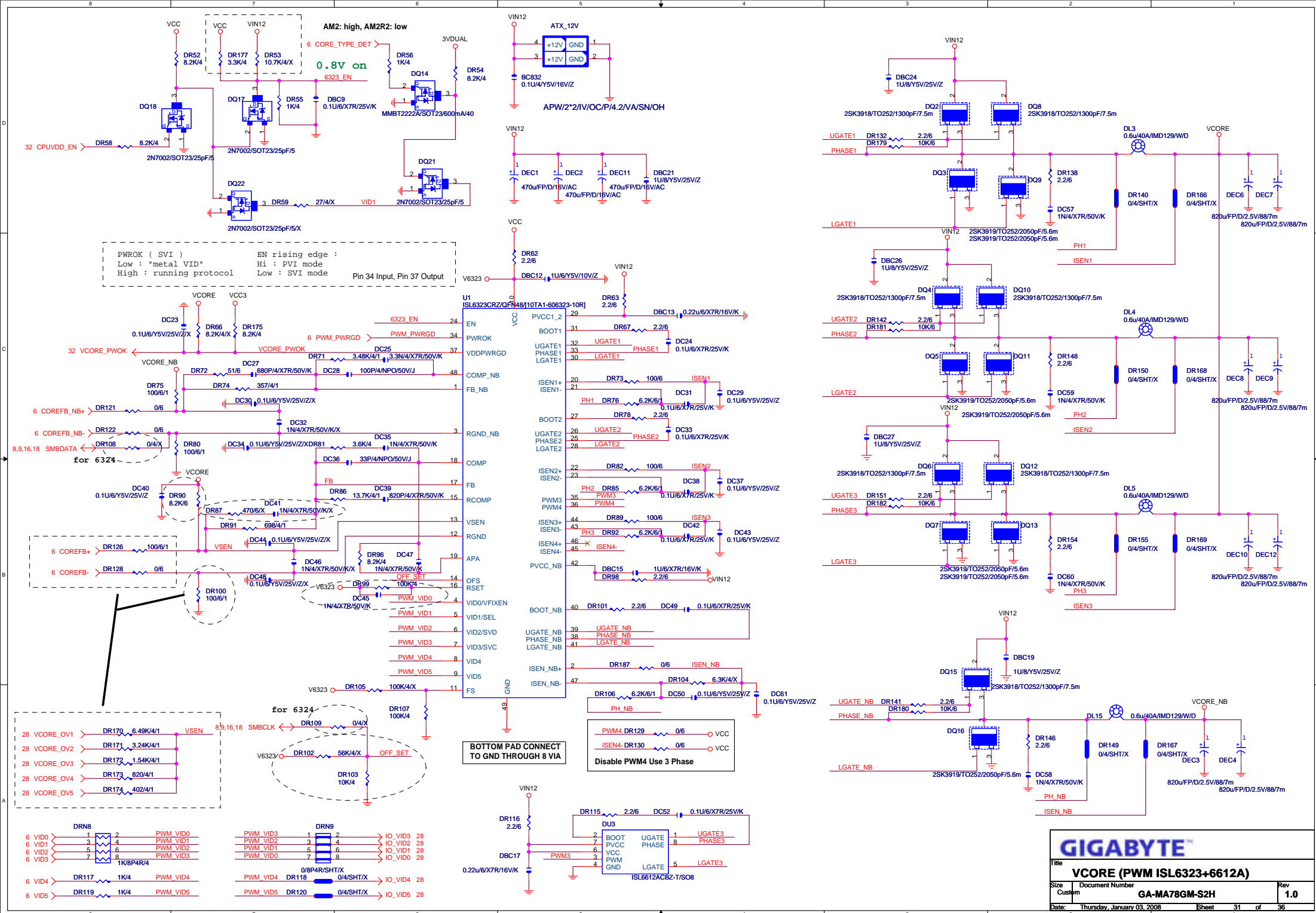
Hardware Monitor circuits

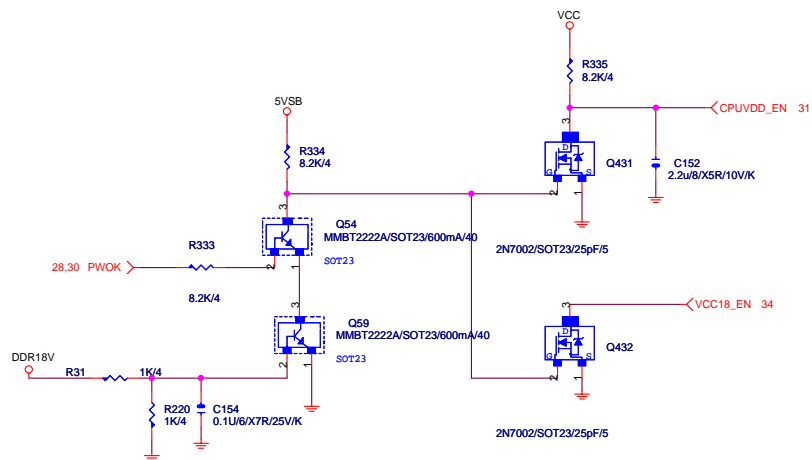
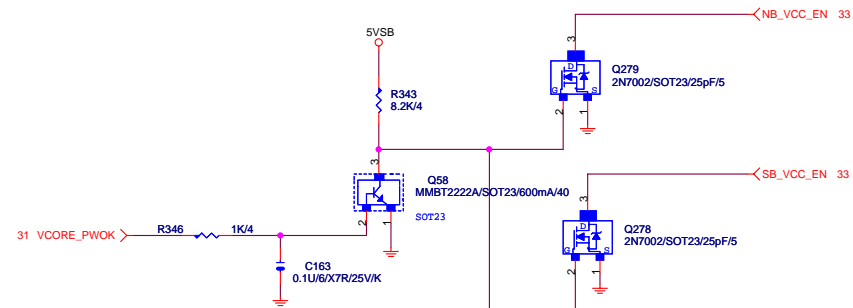
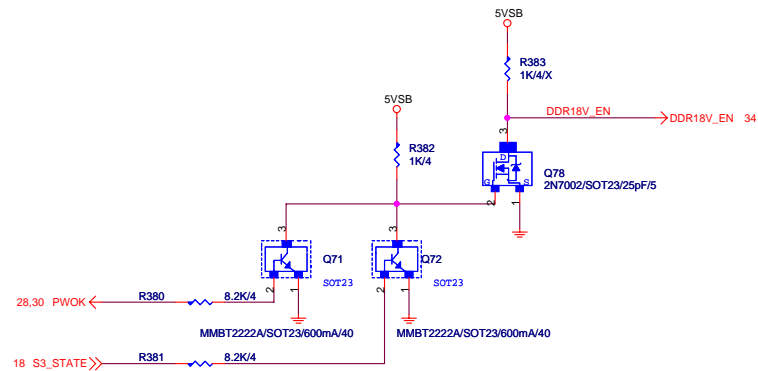




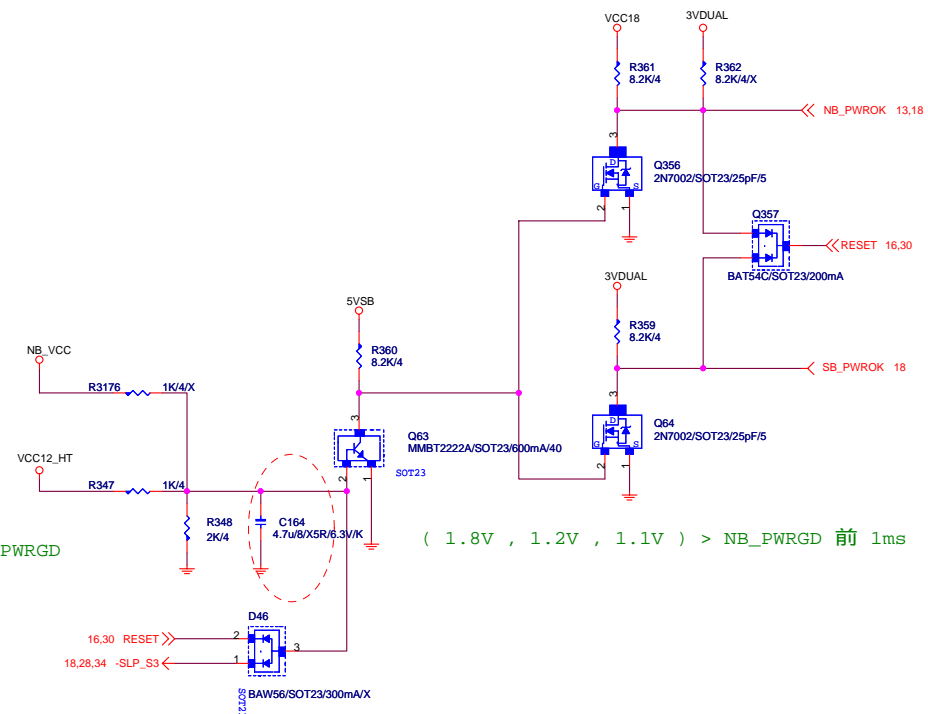
For Seasonic 900W
Power supply
cant Boot issue







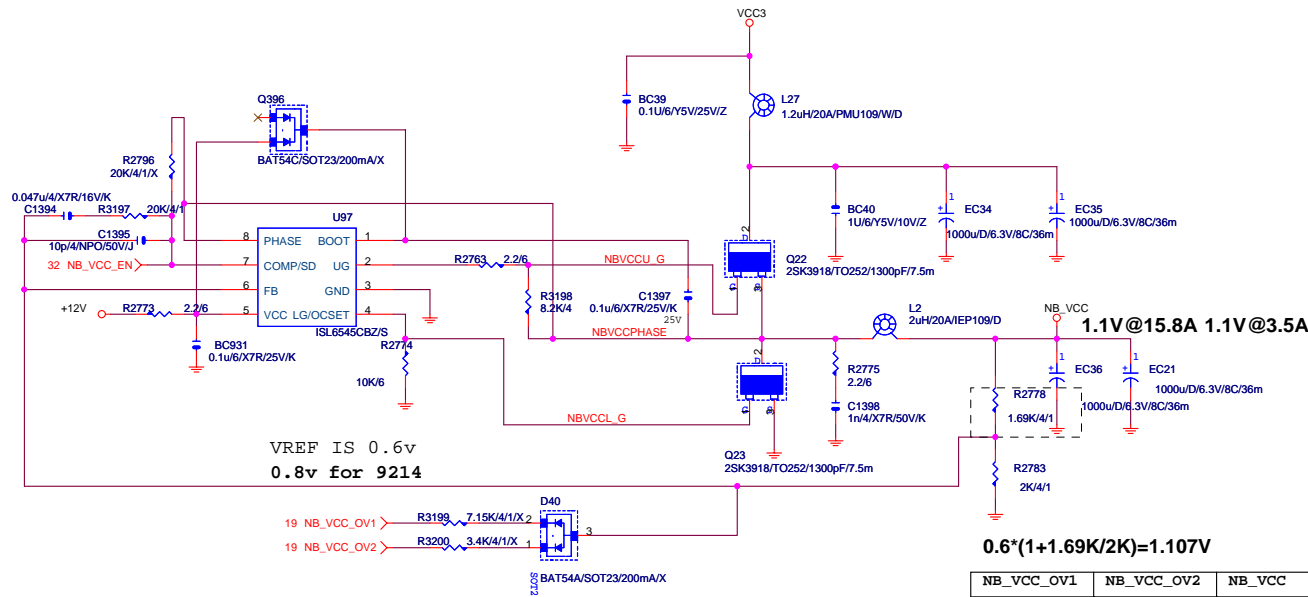
PWOK > NB_PWRGD / SB_PWRGD



(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

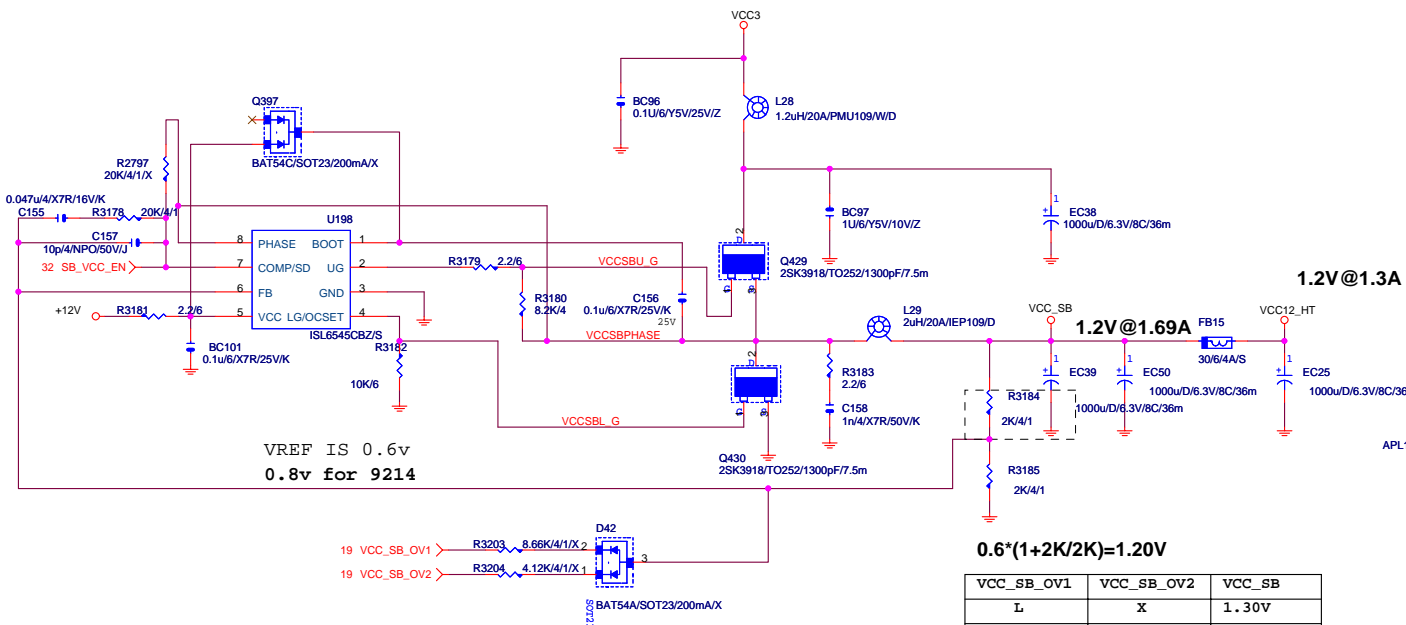
GIGABYTE

Title		
POWER SEQUENCE		
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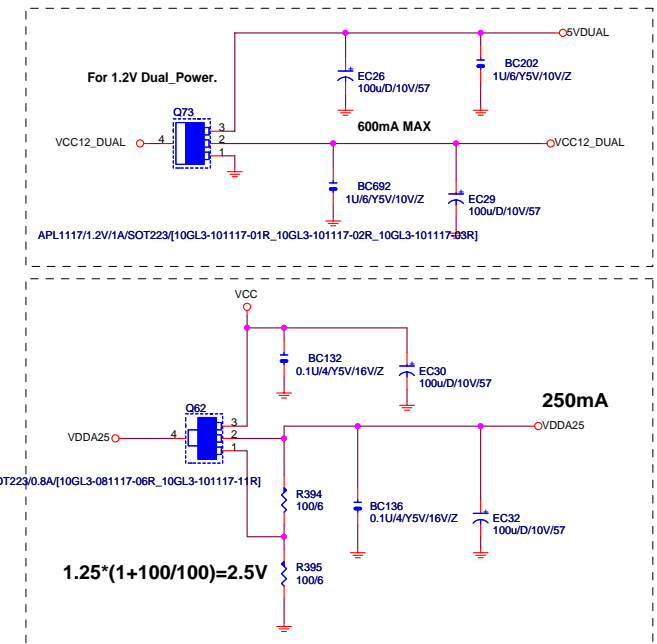
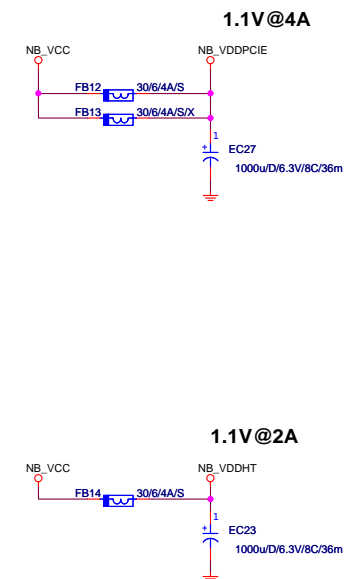
$$0.6 \times (1 + 1.69K/2K) = 1.107V$$

NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V



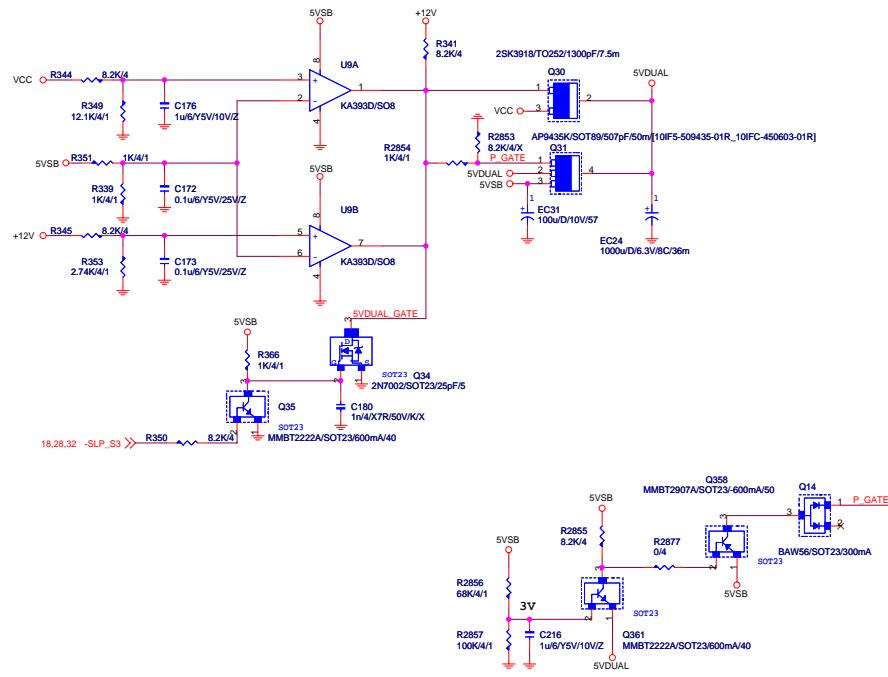
$$0.6 \times (1 + 2K/2K) = 1.20V$$

VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

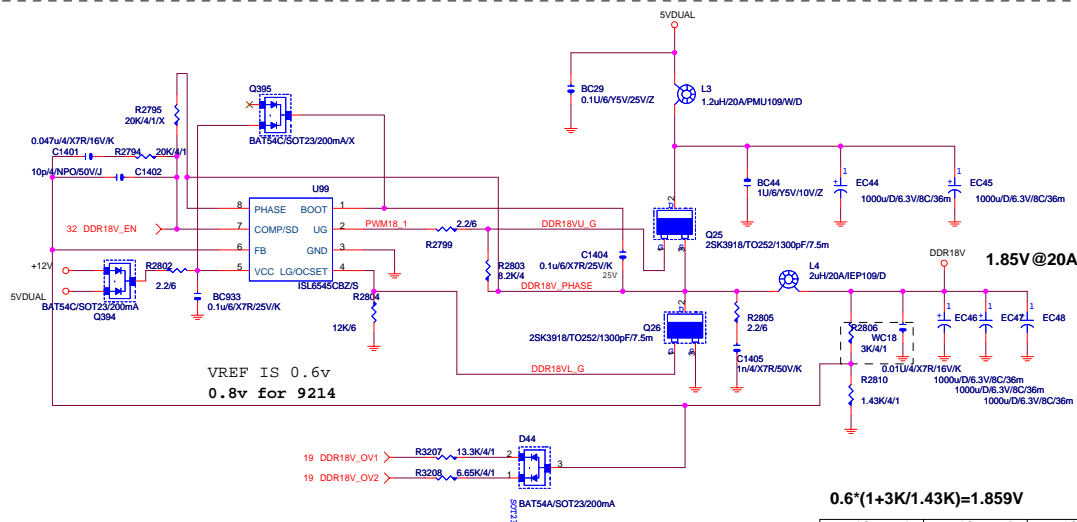
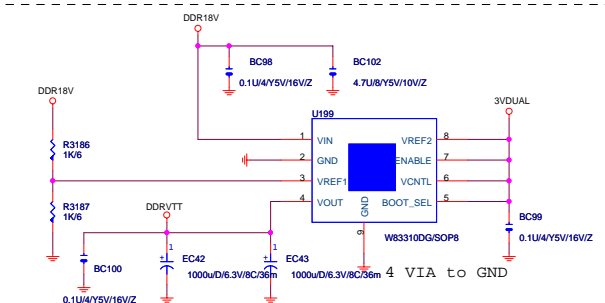
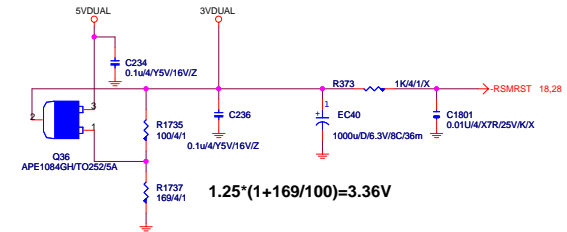


GIGABYTE

5VDUAL

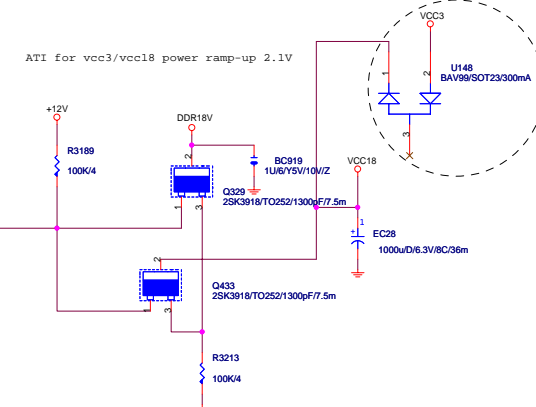


3VDUAL

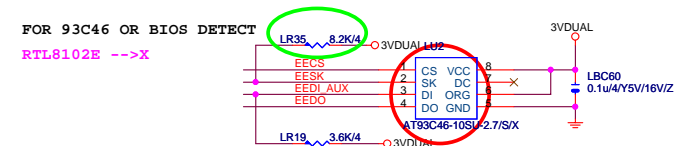
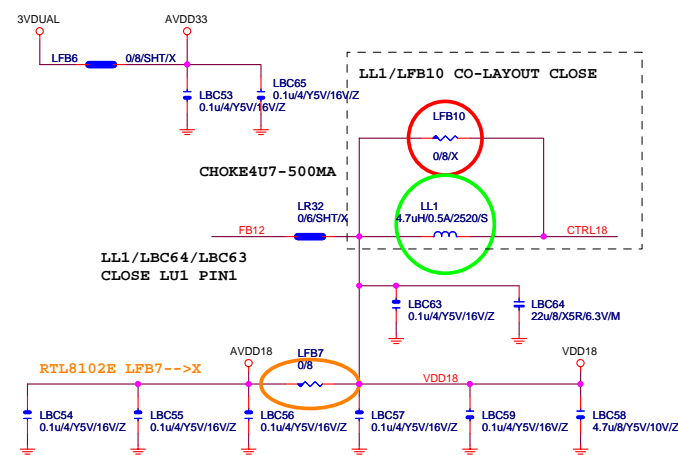
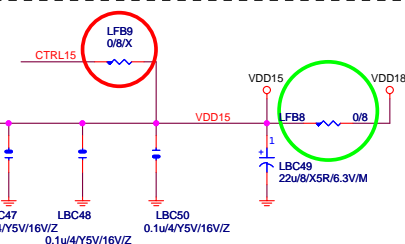
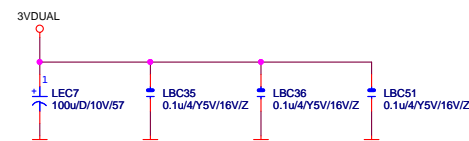
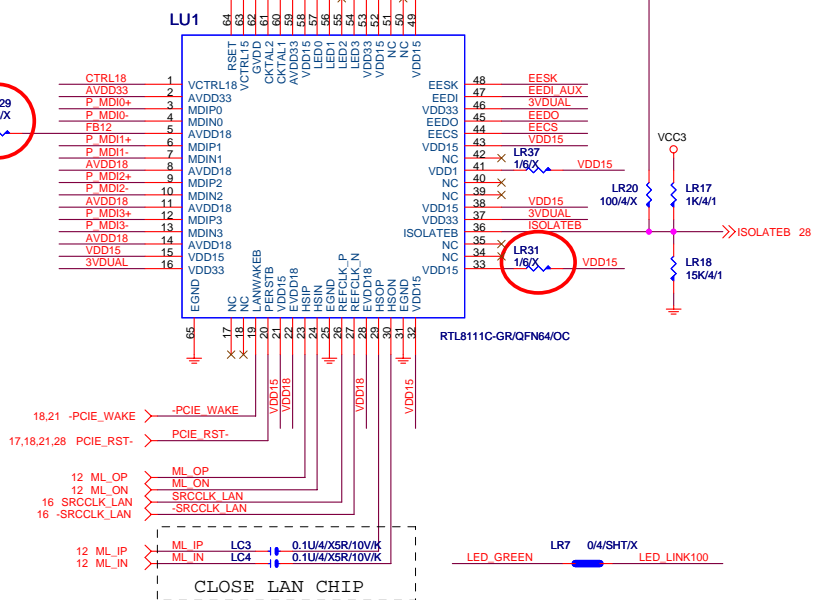
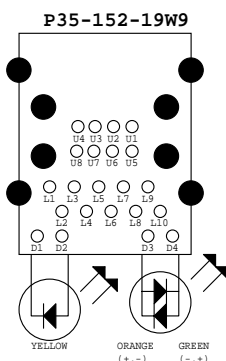
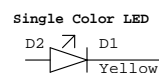
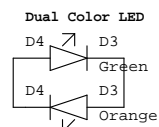
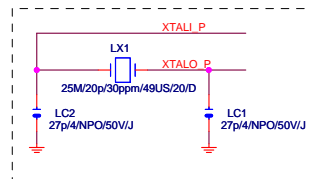
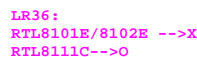
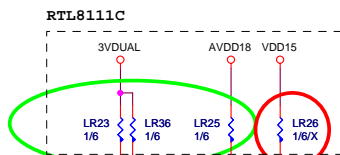
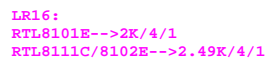


$$0.6 \cdot (1 + 3K/1.43K) = 1.859V$$

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V



PCIE-1G LAN



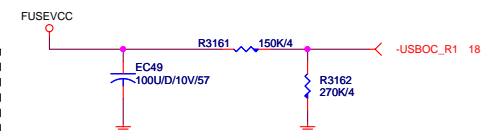
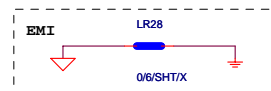
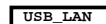
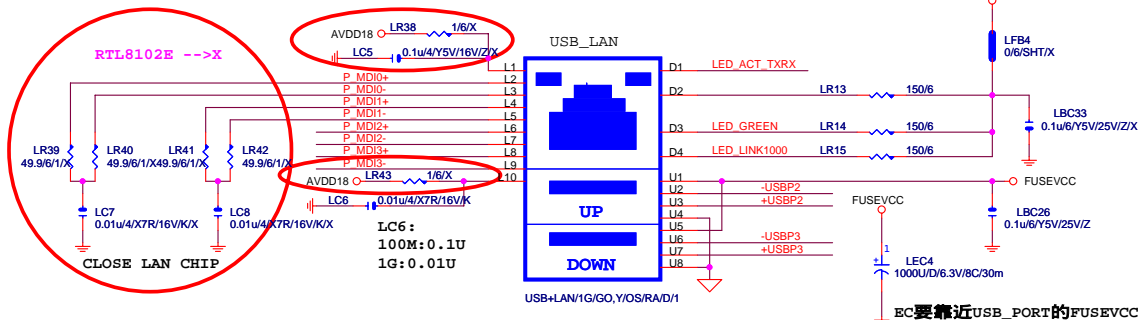
USB_LAN CONNECTOR


```
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8102E:LC5/LC6-->O
RTL8111C:LC6-->O
```

```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
```

1G •USB+LAN/1G/GO Y/OS/PA/D/1

100M:USB+LAN/100/GO,Y/OS/RA/D/1



				
Title				
REALTK RTL8111C/8101E				
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